
Application of micromachining technology for bio-inspired and pressure sensing microsystems

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A thesis submitted for the degree of Doctor of Philosophy.
The University of Edinburgh.
December 2007



Abstract

The main body of this thesis focuses on the fabrication of a micro-electro-mechanical (MEM) air flow sensor for integration with a large scale integration (LSI) neuron circuit and a robot. The proposed MEM sensor consists of: a) Wheatstone bridge circuits made of a patterned metallisation and p-type boron doped microfeatures implanted in n-type single crystalline silicon, b) silicon cantilever beams that are integrated with the Wheatstone bridge circuits, and c) out of plane flaps that are integrated at the free end of silicon cantilever beams. The drag that acts across the flaps when wind moves would cause a torque to appear across the cantilevers, resulting in a mechanical deformation. The mechanical deformation would be transduced by the piezoresistive p-type Wheatstone bridge circuits, which are fabricated on the cantilever beams, in an electrical offset voltage.

The p-type piezoresistive Wheatstone bridge microfeatures are fabricated by boron implantation in n-type single crystalline silicon, forming p-n junctions. Patterned metallisation has been integrated with the boron doped microfeatures and the circuits have been characterised by electrical probing. The electrical circuits and the microcantilever beams have been fabricated on the device layer of silicon on insulator (SOI) wafers. This is followed by release of the microstructures by a bulk micromachining step where the silicon handle wafer and the buried silicon oxide of the SOI wafer, beneath the pre-defined cantilever beams, has been removed. However, devices fabricated in the first design iteration did not meet the specifications and therefore could not be integrated with the LSI neuron circuit. In an attempt to address this issue, the MEM device has been redesigned to meet the specifications. For the fabrication of out of plane flaps, the plastic deformation magnetic assembly (PDMA) has been developed. This method relies on the release of composite structures consisting of a metallic seed layer and an electrodeposited nickel-iron permalloy on top of the seed layer. The structures are released by etch of an underlying sacrificial layer; subsequent exposure of the released structures to a magnetic field results in out of plane deformation of the released flaps.

The final part of this thesis focuses on amorphous silicon carbide thin films and investigation of their suitability for application in SiC membrane based pressure sensors. As amorphous SiC films have been found to not be robust, circular membranes of thermally grown polycrystalline 3C-SiC films for application in absolute pressure sensing devices have been fabricated. Boron doped polycrystalline silicon strain gauges in half active wheatstone bridge arrangement have been integrated with SiC released membranes to transduce pressure induced mechanical deformation of the membranes into an electrical signal. The fabricated devices have been assembled and tested by General Electric. The limiting factor in the performance of the devices at thermal loading has been thought to be a result of the difference in the thermal expansion coefficients of the materials that constitute the pressure sensors. These differences cause thermal stresses and unstable membrane performance.

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Acronyms and abbreviations

Artificial hair cell	AHC
Deep reactive ion etch	DRIE
Inductively coupled plasma	ICP
Large scale integration	LSI
Metal oxide semiconductor field effect transistor	MOSFET
Micro electro mechanical	MEM
Plasma enhanced chemical vapor deposition	PECVD
Low pressure chemical vapor deposition	LPCVD
Reactive ion etch	RIE
Scanning electron microscope	SEM
Silicon on insulator	SOI
Tetramethyl ammonium hydroxide	TMAH
X-ray photoelectron spectroscopy	XPS

Chapter 1

Introduction

This chapter introduces the reader to micro-electro-mechanical systems (MEMS) with the main focus on air flow sensors. Such MEMS may be designed to resemble the functionalities of hair cells found in biological systems and perform various functions such as sensing vibration, flow, and sound. MEM artificial hair cell (AHC) systems are potentially attractive components in bio-mimetic applications, where they are integrated with electronic circuits and robots to construct biologically inspired systems. The aim of this project is the fabrication of an air flow MEM sensor that resembles the functionalities of the hair of the cricket, and its integration with a neuron large scale integration (LSI) circuit and a robot.

In addition, this chapter introduces the reader to silicon carbide and some of its applications in micro-electro-mechanical sensors for operation in harsh environments. The potential benefits of implementing silicon carbide to achieve reliable performance of sensors in harsh environments are explained.

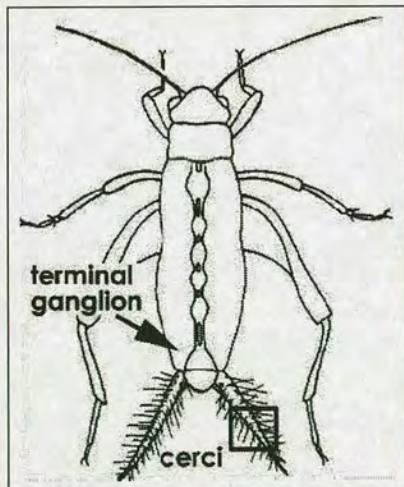
1.1 Motivation - behavioral studies of the cricket

This section gives an introduction to biological and bio-inspired systems and explains our group's motivation for research in this field.

The emerging field of biomorphic sensors and robots includes those artificial devices that borrow biological principles. Research in this field draws motivation from the fact that the performance advantages offered by naturally evolved biological systems could be captured and utilized, leading to sensory devices with superior capabilities. Such robots could imitate the locomotion principles, actuation and navigation capabilities of animals. Such automation and built-in intelligence could assist in the development of superior robots that could be even used in the exploration of other planets [1]. Robots that integrate bio-inspired sensors and neuron computational models could assist scientists to test hypotheses regarding the neuronal control and the behavior of the animals.

Living organisms have developed sensory cells that respond to environmental changes and translate the acquired information into an impulse sequence that is conveyed through the nervous system. The aggregate information generated by the sensory cells is integrated in the nervous systems, it is decoded and eventually controls the action of organisms. However, increasing complexity of organisms leads to increasing complexity of the nervous system and compared to humans, insects are much simpler organisms rendering their study less complex [2]. Insects have a small number of neurons that can be individually identified and characterised and therefore, it could be possible to isolate the neurons of interest and build computational models based on the behavior of the insects [3].

Insects, including the cricket, have developed sensory hairs with lengths ranging from tens of microns to less than two millimeters that are sensitive to air flow. The filiform hairs on the cerci of the cricket perform various roles and can be a source of inspiration for artificial biomorphic systems [4]. A top view of the cricket and the cerci, where filiform hair are attached, can be seen in figure 1.1a and a scanning electron micrograph of a section of the cerci with attached filiform hair can be seen in figure 1.1b.



(a) The cricket as seen from above.



(b) Magnified view of the cercus.

Figure 1.1: a) Diagram of the cricket (top view), and b) SEM image of the cerci showing the filiform hairs. Taken from [4].

Each cercus of the cricket is about 10 mm long [5] and carries a large number (1000 [6] to 2000 [4]) of filiform hairs and a neuronal mechanoreceptor at the base of each hair [7]. When a hair deforms, its corresponding sensory neuron produces a sequence of spikes which are processed by the nervous system of the cricket [8]. The sensitivity of the wind receptors is remarkable

and researchers have estimated that mechanical energy of 4×10^{-21} Joule at 27°C is adequate to trigger sensory cells [9].

The thread like hairs appears to have multi functional roles. For example, they provide a map of the air-flow in the region of the terminal ganglion with great accuracy and precision [4] and therefore, it is believed that they assist the insect in detecting subtle air motions caused by predators, hence enabling the cricket to take an evading action. Furthermore, the sensory hairs of the cricket are sensitive to low frequency particle oscillation, effectively acting as directional acoustic receptors [10].

1.2 Aim of this project

This project will assist in the behavioral study of the cricket; the role of filiform hairs in the detection of wind flow caused by predators and the evasive action taken by the cricket will be examined using a cricket bio-inspired robotic system. An overview of the robotic system is shown in figure 1.2.

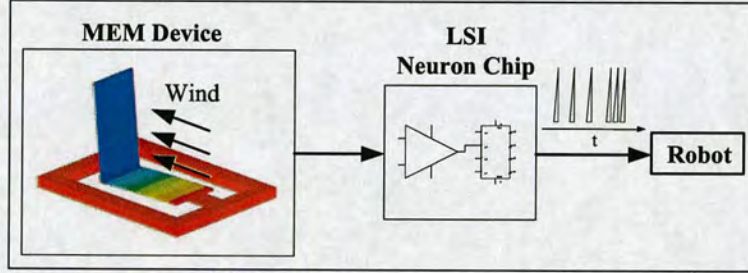


Figure 1.2: Overview of the cricket bio-inspired robotic system.

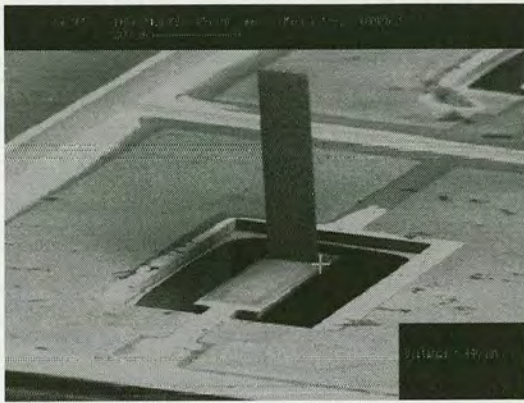
The system consists of: a) micro-electro-mechanical artificial air hair cells (MEM AHCs) of variable length that produce electrical signal when stimulated by air, b) a large scale integration neuron circuit that detects the electrical signal from the MEM AHCs and produces electrical spikes, and c) a computational model that processes the electrical spikes from the LSI circuit and delivers a behavioral model that controls a robot. This thesis focuses on the fabrication of the MEM sensor that responds to wind stimulation and produces an electrical signal that can be processed by the LSI neuron circuit.

1.3 Bio-inspired MEM flow sensors

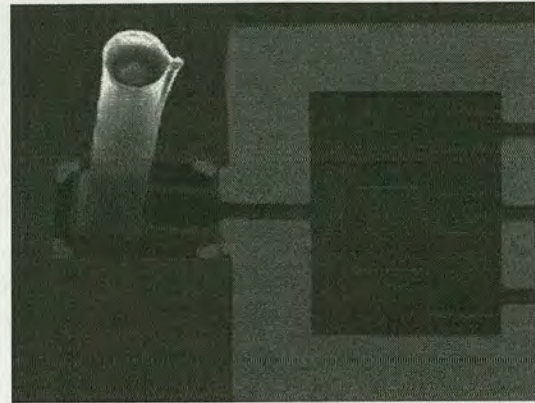
To gain an understanding of the current MEMS air flow sensors and technology, some MEM devices developed for applications in bio-mimetic systems are reviewed in this section.

Zhifang Fan *et al.* from the University of Illinois at Urbana-Champaign have been inspired by water flow sensing cilia found on fish and have fabricated artificial hair cell sensors operating underwater for application in robotics and military applications [11]. An artificial hair cell consisting of a silicon micromachined cantilever beam and an out of plane flap can be seen in figure 1.3a. The illustrated cantilever beam has been released by deep, bulk etch of the wafer underneath the cantilever beam and the out of plane flap has been fabricated using the plastic deformation magnetic assembly (PDMA) method. As air flows, drag appears across the out of plane flap transferring torque to the released end of the cantilever beam, subsequently causing bending of the structure. A p-type piezoresistor has been integrated at the neck of the cantilever beam and transduces mechanical deformation of the cantilever beam due to air-flow, to change in the electrical resistance of the piezoresistor, which is detectable by electronic equipment. For the fabrication of out of plane flaps, the plastic deformation magnetic assembly (PDMA) method has been developed; this method relies on the release of composite structures consisting of a metallic seed layer and electrodeposited nickel-iron permalloy on top of the seed layer. Etch of the underlying sacrificial layer releases the structures and subsequent exposure of the released structures to magnetic field results in their out of plane deformation. The main advantage of the PDMA method is that out of plane flaps of variable length can be achieved as final structures. However, this process requires the characterisation of nickel-iron permalloy electrodeposition and the investigation of a reliable sacrificial etch and release method.

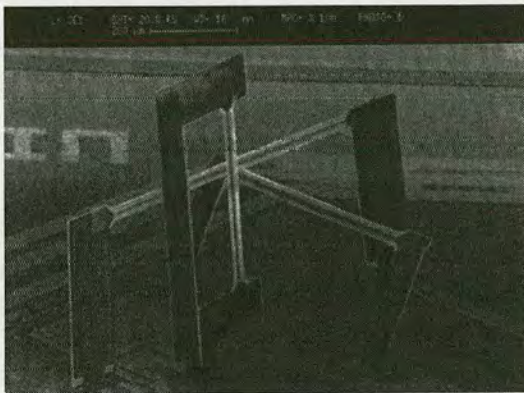
Chen *et al.* [12], also from the University of Illinois at Urbana-Champaign, have fabricated an air flow sensor based on a cantilever with an integrated piezoresistor, but have used thick patterned SU-8 photoresist to fabricate out of plane cilia like structures, as can be seen in figure 1.3b. To fabricate these structures, a thick SU-8 film is coated on the wafers and subsequently the resist is exposed in a mask aligner and developed, prior to the release of the cantilever beams. Although SU-8 photoresist requires more complex baking methods than conventional positive photoresists, it remains a simpler approach compared to the PDMA. The disadvantage of the SU-8 approach is that the length of the final structures is defined by its thickness, which is obtained in the spin coating process. Because the thickness of the SU-8 photoresist obtained by spin coating is uniform across the wafer, it is not possible to obtain final out of plane structures



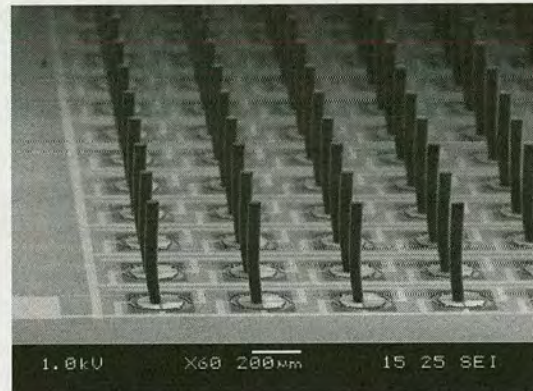
(a) A flap fabricated by the PDMA method on a released silicon cantilever beam with a piezoresistive strain gauge on the neck of the cantilever [11].



(b) Patterned SU-8 photoresist tube on a released silicon cantilever beam with a piezoresistive strain gauge on the neck of the cantilever [12].



(c) Out of plane hot-wire anemometers fabricated by the PDMA method [13].



(d) Patterned SU-8 photoresist tubes on released silicon nitride disks with capacitive readout [14].

Figure 1.3: Different types of bio-inspired MEM flow sensors.

of variable length by a single coat-exposure step and multiple resist coating and exposure cycles are necessary to obtain out of plane structures of variable length on a wafer/device.

Another type of air flow sensors, namely hot-wire anemometers (HWA), utilize a thermal element (thermistor) that serves as both a Joule heater and a temperature sensor. When power is applied to the thermistor at zero air flow rate, the thermistor acquires steady state temperature and resistance. As the air flow is modified, the thermal element will experience forced cooling, hence its resistance will be modified accordingly. By monitoring the resistance -modulated by air flow- the stream speed of the surrounding air can be deduced. Chen *et al.*, from the University of Illinois at Urbana-Champaign, have employed the PDMA method to fabricate permanently deformed non-movable out of plane HWAs, as can be seen in figure 1.3c, which successfully sense flow of surrounding air [13]. As these sensors do not include any movable

parts, the fabrication process is simpler compared to the aforementioned cantilever beam based air flow sensors.

The Cricket Inspired perCeption & Autonomous Decision Automata (CICADA) project aims to “transfer knowledge from the sensing-perception-action mechanisms in insects escaping danger to the development of highly integrated artificial life-like miniature systems based on Micro Electro Mechanical Systems (MEMS) and Bio-Electronic technologies” [15]. Krijnen *et al.* have been inspired by the auditory capabilities of the filiform hair of the cricket and have fabricated a MEM system capable of detecting low-frequency particle oscillation, namely sound [14, 16]. A SEM image of the fabricated system can be seen in figure 1.3d and consists of: a) an array of circular silicon nitride disks suspended over electrically conducting silicon substrate, b) metallic electrodes on top of the silicon nitride suspended disks, essentially forming a capacitor, and c) thick SU-8 photoresist patterned in tubular structures on top of the suspended silicon nitride disks. The geometrical parameters have been chosen such that the natural resonance frequency of the structures is $f_{res} \leq 1KHz$. The capacitor, formed by metallic electrodes on top of suspended disks and the underlying electrically conducting silicon substrate, is biased with a high frequency (1MHz) alternating current-voltage source and the capacitive impedance is measured with electronic equipment. When a sound emitting source generates alternating particle oscillation, alternating drag force appears across the artificial cilia, causing the MEM structures to vibrate. As the structures vibrate under the influence of sound, the capacitor’s gap (formed by the disk and the substrate) is modified, thus sound modulation of the capacitive impedance is achieved. When the sound frequency matches the resonance frequency of the MEM artificial hair cells, the vibration amplitude of the structures is maximized. Therefore, by varying the geometric characteristics of the artificial hair (length and diameter) selectivity in 0-1KHz frequency spectrum can be achieved. The advantage of this MEM system is that it is modeled mechanically as an inverted pendulum and, as will be described in chapter 2, resembles closely the characteristics of the filiform hair of the cricket. The disadvantage of this design is that complex electronic equipment is required to drive the MEM system.

In this section bio-inspired MEM air flow sensors found in the literature have been presented. For our project, it has been specified that artificial hair cells of variable length are fabricated and, therefore, the design approach by Zhifang Fan *et al.* has been chosen. In this design the PDMA method is employed to fabricate out of plane flaps of variable length on the free end of released silicon micromachined cantilever beams, as can be seen in figure 1.3a. A piezoresistor

located at the neck of the cantilever beam transduces mechanical deformation of a cantilever beam to change in electrical resistance, which is detected by electronic equipment. The detailed specifications for our MEM system are given in chapter 2.

In the next section the application of silicon carbide in micro-electro-mechanical systems, which is also investigated in this thesis, is discussed briefly.

1.4 Application of silicon carbide in pressure sensors

Silicon carbide (SiC) is a promising material for the development of high-temperature solid-state electronics and transducers, owing to its excellent electrical (high bandgap) and mechanical (good stability at high temperatures) properties. Silicon carbide is grown in high temperature, low pressure chemical vapor deposition (LPCVD) or atmospheric pressure chemical vapor deposition (APCVD) reactors and exhibits polymorphism. Amorphous SiC (*a*-SiC) films can also be deposited by the low temperature plasma enhanced chemical vapor deposition (PECVD) method. The preferred and most common polytype investigated for application in MEMS is 3C-SiC because it can be synthesized directly on silicon wafers whereas 4H-SiC and 6H-SiC synthesize at temperatures above the melting point of silicon. More details on the properties of silicon carbide are given in chapter 7.

Applications of SiC based sensors for operation in harsh environments include monitoring of internal combustion, rocket, turbine engines that could increase the operational efficiency of such systems [17].

Here we are interested in the fabrication of SiC pressure sensors for application in harsh environments. In the final part of this thesis, the suitability of amorphous SiC (*a*-SiC) deposited by the PECVD method for application in MEMS is investigated. Finally, a 3C-SiC thin film deposited on a silicon substrate by the high temperature LPCVD method has been used to fabricate successfully 3C-SiC membranes for application in pressure sensing devices.

1.5 Thesis Overview

This thesis is divided in two main parts. The main body of this thesis (chapters 2-6) focuses on the fabrication development toward a MEM system inspired by the cricket's filiform hairs.

A minor part of the thesis (chapters 7-8) focuses on the investigation of amorphous silicon carbide for application in MEM devices and the fabrication of 3C-SiC thin film membranes for application in MEM pressure sensors. An overview of the structure of the thesis and brief summary of each chapter is made below.

Chapter 2: Background theory. The fundamental background theory on the bio-mechanics of the filiform hair of cricket is presented. The mechanics of materials and the piezoresistive properties of silicon are introduced to the reader. ANSYS simulations are performed to gain insight into the geometrical design parameters and the design trends that optimize the sensitivity of the proposed MEM air flow sensing system. Using analytical calculations the frequency characteristics of the proposed MEM system are estimated and compared with the response of the cricket's wind mechanoreceptors.

Chapter 3: Design, fabrication and characterisation of boron implanted resistors with metallisation. Experimental chapters begin with the development of Wheatstone bridge circuits consisting of p-type boron doped regions in single crystalline silicon. The implanted regions are integrated with metallic electrodes.

Chapter 4: First design iteration: integration of full-active Wheatstone bridge circuits with silicon cantilever beams. Full-active Wheatstone bridge circuits (p-type boron doped microfeatures/metallisation) developed in chapter 3 are integrated with silicon micromachined cantilever beams. The fabricated devices did not meet the specifications and could not be integrated with the LSI neuron chip. In an attempt to address this issue, the MEM device has been redesigned to meet the specifications in chapter 5.

Chapter 5: Second design iteration: integration of half-active Wheatstone bridge circuits with second generation cantilever beams. To allow integration of the MEM device with the LSI neuron chip and also to increase the sensitivity of the MEM devices to air stimulation, the design is re-iterated to include half-active Wheatstone bridge circuits integrated with second generation silicon cantilever beams. A multilevel metallisation process is developed to reduce the number of bonding pads on the final devices.

Chapter 6: Plastic deformation magnetic assembly. The PDMA method is developed for the fabrication of out of plane flaps of variable length. The electrodeposition of nickel-iron permalloy on metallic seed layer is characterised. Release methods, where a sacrificial layer is etched to release overlying composite metallic seed layer – nickel-iron permalloy structures

prior to their deformation, are investigated.

Chapter 7: Relaxation of process-induced surface stress in amorphous silicon carbide thin films using low energy ion bombardment. In this chapter the suitability of PECVD amorphous silicon carbide thin films for application in MEMS is investigated. α -SiC cantilever beams are fabricated using stressed nichrome, PECVD SiO₂ and SiN thin films as masks during etch and release step of the α -SiC microstructures. Severe deformation of the SiC microstructures is observed after removal of stressed SiO₂ mask, due to fabrication induced surface stress. The fabrication induced stress could be relaxed after the removal of the etch mask by low energy ion bombardment in inductively coupled plasma reactor.

Chapter 8: Absolute pressure sensors with silicon carbide and silicon membranes. Absolute pressure sensors fabricated here implement flexible circular membranes made of single crystalline silicon or thermally grown 3C-SiC. The membranes deform mechanically when a differential pressure appears across their surfaces. The method used to detect changes in a membrane's deformation involves strain gauges that are positioned on top of the membrane. The fabricated devices have been assembled and tested by General Electric, and it has been found that under thermal loading the devices exhibit unstable performance.

Chapter 2

Background Theory

In section 2.1 the literature on the wind mechanoreceptors of the cricket is reviewed; the mechanical systems that are used to model the receptors as well as the response of the receptors to air stimulation are presented. Section 2.2.1 provides a brief introduction to theoretical models of fluid dynamics and the drag of air on flat objects. Next, the mechanics of materials (section 2.2.2), and the silicon elastic (section 2.2.3) and piezoresistive properties (section 2.2.4) are presented. The concept of stress concentration regions are presented (section 2.2.5) and ANSYS finite element simulations of cantilever beams with stress concentration regions are performed (section 2.2.6). Next, the Wheatstone bridge circuit is briefly discussed in section 2.2.7. The approximate frequency response of the proposed MEM cantilever-flap system is calculated and is compared with the frequency response of the cricket's wind mechanoreceptors in section 2.2.8. In section 2.3 the specifications of the MEM device are listed and the chapter closes with conclusions in section 2.4.

2.1 The model of the cricket wind mechanoreceptors

Authors Kumagai, Shimozawa and Baba have been researching extensively the mechanical model of the cricket hairs. In three publications, the authors have shown that the hair of the cricket can be modeled as a mechanical inverted pendulum with a cone-shaped solid shaft, supported at its base with a spring and a damper [18–20], shown in figure 2.1. The inverse pendulum is a typical second order system that can be described by the second order nonhomogeneous differential equation 2.1.

$$I \cdot \frac{d^2\theta(t)}{dt^2} + R \cdot \frac{d\theta(t)}{dt} + S \cdot \theta(t) = N(t) \quad (2.1)$$

where I is the moment of inertia of the hair, R is the torsional resistance, S is the spring stiffness and θ is the radial deflection of the shaft due to effective torque N that is induced on the shaft by air motion. Because the effective torque is not known, the authors have used Stoke's mechanical impedance of a cylinder in oscillating fluid to derive the torque N acting on the hair.

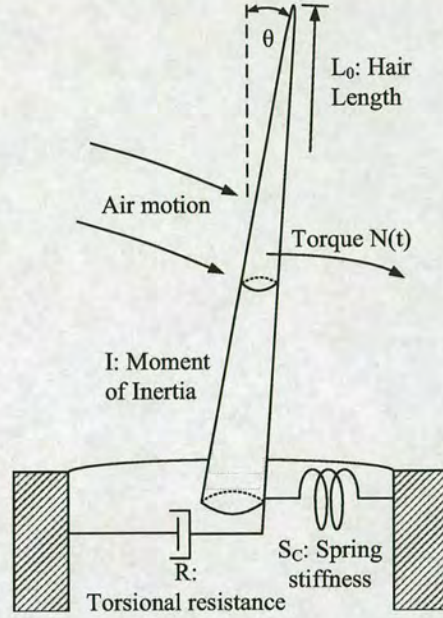


Figure 2.1: *The mechanical model of a wind mechanoreceptor. Reproduced from [20].*

Using experimental procedures, the authors have characterised the radial deflection degree of hairs as a function of frequency from 0 to $\sim 1\text{KHz}$ [19]. The experimental data of the radial deflections and the applied torque N (calculated from Stoke's model) have been curve fitted to derive the parameters I , R and S of the differential equation 2.1 [20]. The differential equation parameters as a function of frequency are plotted in figure 2.2. It is observed that between short ($160\mu\text{m}$) and long ($1500\mu\text{m}$) hairs the spring stiffness varies by approximately 1.5 orders of magnitude, the torsional resistance by 2.5 orders of magnitude and the moment of inertia varies by 4 orders of magnitude(!).

If we set the torque N to zero, equation 2.1 becomes homogeneous and can be solved using known parameters I , R , S . Solving the homogeneous equation results in general solutions that represent the natural frequency response of the mechanoreceptors. A general solution has been calculated numerically in Matlab; it has been found that the natural frequency response of a $1000\mu\text{m}$ long hair is a low pass filter with cut-off frequency at approximately 1KHz . This can be seen in figure 2.3, curve (a).

At low frequencies, the boundary layer becomes very thick and short hairs, deeply immersed in this layer, become insensitive. Long hairs, which are sensitive to low frequencies, have a high moment of inertia and become insensitive to high frequency sound waves. The effect of the boundary layer and the frequency dependent air-hair friction coefficient D result in a torque N

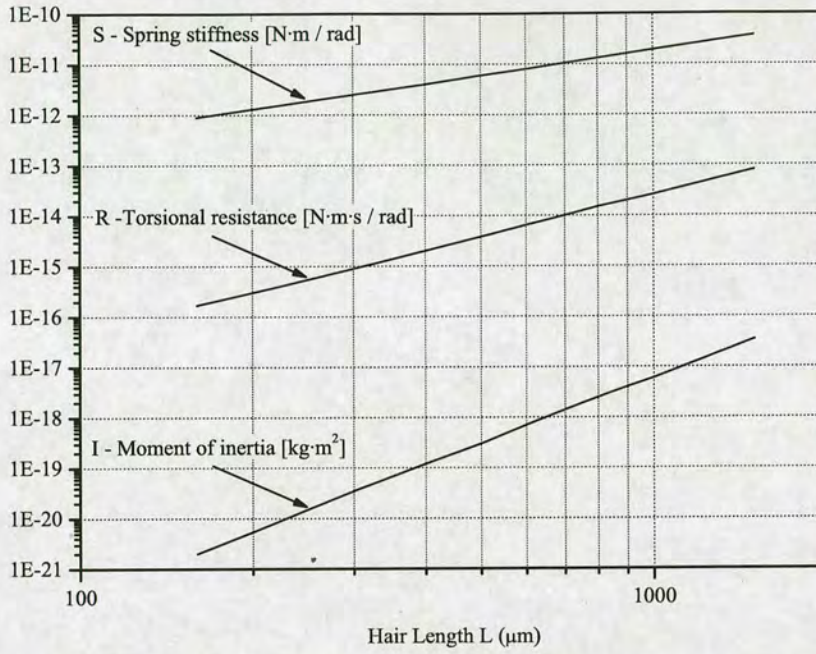


Figure 2.2: Logarithmic plot of the moment of inertia, torsional resistance R and spring stiffness S versus receptor shaft length.

with high-pass filtering properties.

Summing the high-pass (from the torque N) and low-pass (natural frequency) response gives the complete solution to the non-homogeneous differential equation 2.1. The summation of low-pass and high-pass filters implies that the frequency response of the wind mechanoreceptors is effectively band-pass. The band-pass filtering properties of the wind mechanoreceptors with 1000-1500 μm long hairs have been reproduced here using data from the literature and can be seen in figure 2.3, curve (b). In the same figure is shown how the numerically calculated natural low-pass frequency response of the mechanoreceptors (curve (a)) is modified into a band-pass response (curve (b)), due to the aforementioned effect of the torque N . Also, in figure 2.3, curve (c), is shown the experimentally derived frequency response of a 300 μm long hair. It is observed that in low frequencies the radial deflection of long hairs has larger magnitude compared to short hairs. As the frequency increases this inverts and the radial deflection of short hairs becomes larger compared to the radial deflection of long hairs.

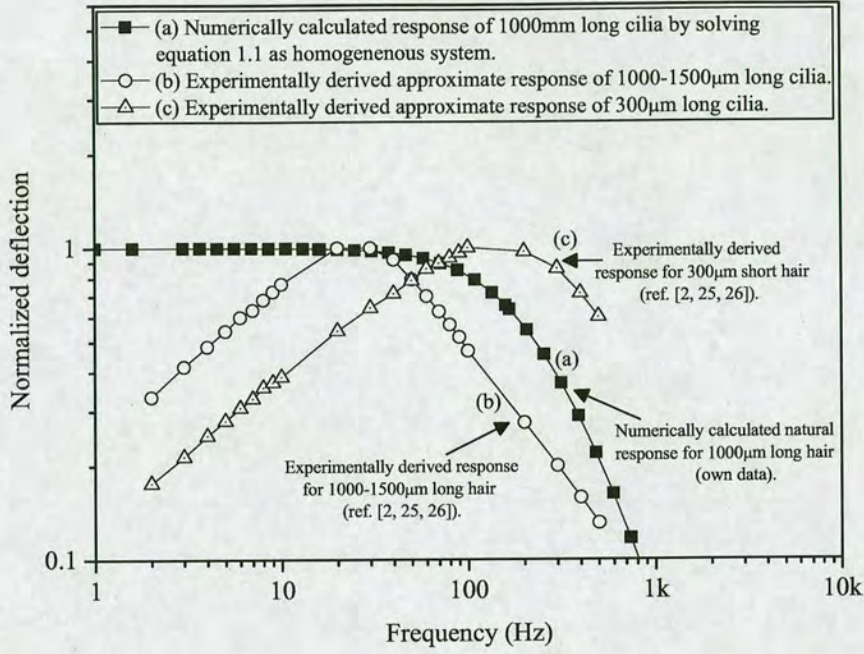


Figure 2.3: Frequency response of mechanoreceptors: a) numerically calculated - 1000 μm hair length, b) experimentally derived - 1000-1500 μm hair length, c) experimentally derived - 300 μm hair length.

The frequency selectivity of the mechanoreceptors cause them effectively to act as directional sound receptors that capture low frequency sound waves ($<1\text{kHz}$) emitted from small bodies with size $\leq 2\pi\lambda$, where λ is the wavelength of the sound wave [21]. The measured best frequencies are 30-60Hz for 1000-1500 μm long hairs, 50-80Hz for 700-1000 μm long hairs and 100-200Hz for 160-700 μm long hairs. The gain slopes are 10-20dB/decade for short hairs at low frequencies and up to -30dB/decade for 1000-1500 μm long hairs at high frequencies.

Assume that we expose long hairs (1000-1500 μm) to a sound source emitting a sine wave with frequency $f_L = 45\text{Hz}$, matching the best frequency of long hairs. The sine wave is expressed as $\sin(2 \times \pi \times f_L) = \sin(282.6) = \sin(\omega)$. The rate of change, or acceleration of this function is expressed by its first derivative: $\frac{\sin(\omega)}{d\omega} = \cos(\omega)$. We follow the same reasoning for short hairs (160-700 μm) exposed to a sound source emitting a sinusoidal wave with frequency $f_S = 150\text{Hz} = 3.33 \times f_L$, matching the best frequency of short hairs. This sine wave is expressed as $\sin(2 \times \pi \times f_S) = \sin(2 \times \pi \times 3.33 \times f_L) = \sin(3.33 \times \omega)$ and the acceleration

of the function which is expressed by its first derivative is: $\frac{\sin(3.33 \times \omega)}{d\omega} = 3.33 \times \cos(3.33 \times \omega)$. It is observed that the acceleration of the sine wave at 150Hz (best frequency of short hairs) is 3.33-fold the acceleration of the sine wave at 45Hz (best frequency of long hairs). This is the reason why, in the literature, the frequency selectivity of short and long hairs sometimes is referred to as ‘acceleration sensitivity’ and ‘velocity sensitivity’ respectively [5].

In this project the acoustic properties of the cricket are not of interest. Dr. Barbara Webb, our collaborator at the School of Informatics, is interested in the role that acceleration and velocity sensitive short and long hairs respectively may play in the evading action of the cricket. Subsequently, the main specification for this project has been the fabrication of a MEM wind flow sensor that implements out of plane flaps of variable length that ‘mimic’ the hair of the cricket. However, the hair length alone cannot introduce frequency selectivity properties, hence length dependent sensitivity to velocity or acceleration.

To mimic precisely the cricket’s wind mechanoreceptors, a MEM system should resemble the aforementioned mechanical inverted pendulum shown in figure 2.1 and should be described by the second order differential equation 2.1 with variables I , R , and S shown in figure 2.2. The natural frequency response of the system should possess low-pass frequency ($\leq 1\text{KHz}$) filtering properties. As mentioned in the introduction, Krinjen *et al.* have managed to fabricate released MEM disks with long SU-8 photoresist shafts positioned on top of released silicon nitride disks [14, 16]. These devices resemble the aforementioned mechanical inverse pendulum, resonate at sub-1KHz frequencies and achieve the objective of mimicking the auditory capabilities and frequency response of the cricket’s mechanoreceptors, with ‘velocity’ and ‘acceleration’ sensitivity.

2.2 Transferring from biology to silicon

In this section fluid dynamics properties relevant to this project and issues regarding its applicability to our project are discussed (section 2.2.1). Next, brief information on material mechanics (section 2.2.2) as well as the elastic (section 2.2.3) and piezoresistive properties (section 2.2.4) of silicon are presented. The concept of stress concentration region is given (section 2.2.5) and ANSYS finite element modeling simulations are performed in order to determine the optimized design parameters (section 2.2.6). Next, the Wheatstone bridge circuit is presented and potential implication regarding its use in this project are discussed (section 2.2.7). Finally

the calculated approximate frequency response of the proposed MEM system is presented and compared with the response of the mechanoreceptors (section 2.2.8).

2.2.1 Fluid dynamics and drag on a flat plate

Fluid dynamics belongs to a different scientific discipline and to estimate the drag that air motion would cause to the devices here would require researchers with expertise in this subject. Since it has been requested to simulate the response of MEM devices to air motion, an approach is made here to understand the fluid dynamic theory relevant to our application.

A fundamental characteristic of fluids is that the velocity of the fluid at a surface is zero. This results in a region close to the solid's surface where the fluid velocity increases from zero to the velocity of the main stream. This region is called the *Boundary Layer* and its thickness is by definition equal to the distance between the surface of the solid and the point where the flow velocity reaches 99% of the main stream velocity. The Reynolds number is used as a rule that determines whether the flow is laminar or turbulent, and is defined by equation 2.2.

$$Re_x = \frac{u_\infty \times x}{\nu} \quad (2.2)$$

where u_∞ is the velocity of the fluid in the main stream, x is the distance along the flat surface and ν is the kinematic viscosity of the fluid. For values of $Re_x < 10^5$, the flow is laminar and very stable. The transition from laminar to turbulent flow occurs for Reynolds numbers $10^5 < Re_x < 2 \times 10^6$, and for $Re_x > 2 \times 10^6$ the flow is turbulent. For a flat surface, the thickness δ of the boundary layer by Blasius's solution is given by equation 2.3.

$$\delta = \frac{6.01 \times x}{\sqrt{Re_x}} \quad (2.3)$$

The MEM wind sensor will be fabricated on a 1cm^2 die. The device will operate at room temperature, at air velocities ranging from 0.1m/s to 3.9m/s. In these conditions, the kinematic viscosity of air is equal to $\nu = 1.37 \times 10^{-5}\text{m}^2/\text{s}$. If we combine these parameters with equation 2.2, we can calculate the regime of Reynolds numbers for the operating conditions of our device. The resulting values are in the range $6.62 < Re_x < 2582$. The lowest value occurs at the beginning of the surface ($x = 1\text{mm}$) and at the lowest air speed (0.1m/s), while the maximum value occurs at the end of the surface ($x = 10\text{mm}$) and at the highest air speed (3.9m/s). For such low Reynolds numbers laminar air flow is expected.

When the moving fluid meets an object that is not parallel to the flow, a differential pressure develops across the object. The amount of a drag that an object generates is expressed by the drag coefficient C_D of the object, given by equation 2.4.

$$C_D = \frac{F_D}{\frac{1}{2} \times \rho \times u_\infty^2} \quad (2.4)$$

where F_D is the total drag force, ρ is fluid density, and u is the fluid velocity. Although equation 2.4 has been used in the literature to derive the drag on MEMS air sensors [11], it does not take into account the effects of the boundary layer. Therefore it is not known whether equation 2.4 is applicable to our system parameters and, therefore, the accuracy of any calculations cannot be determined.

2.2.2 Mechanics of materials

Stress and strain are two of the most fundamental concepts of solid matter and are illustrated in figure 2.4.

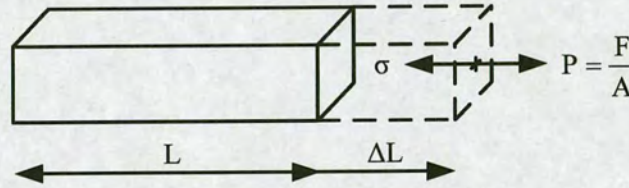


Figure 2.4: Bar in tension.

When a pressure P is applied along the right end of the bar while maintaining the left end fixed, an axial elongation ΔL is caused. The resultant strain is defined in equation 2.6.

$$\epsilon = \frac{\Delta L}{L} \quad (2.5)$$

Equilibrium is achieved when a stress σ acts to counterbalance the applied pressure. In figure 2.4 the stress acts along the axis of the bar and is defined as axial stress. For small strains, stress and strain are linearly related by Hooke's law, defined in equation 2.6.

$$\sigma = E \times \epsilon \quad (2.6)$$

where E is the Young's Modulus of the material in Pascal units. When the bar is elongated, it is in tension and the stress is tensile. If the pressure had the opposite direction, the bar would be in compression and the stress would be compressive. As mentioned previously, in this project the fabricated cantilever beams will be subject to torque at their free end. In this case a constant moment per unit length is applied across the cantilever and the cantilever is said to be in pure bending. When the free end is laterally deflected due to an acting moment M as shown in figure 2.5, the bulk of the cantilever above the neutral axis O (where the stress is equal to zero) is in tension, while the other half is in compression. The maximum stress/strain occurs at the surfaces of the structure.

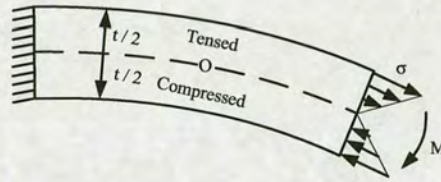


Figure 2.5: Cantilever beam in pure bending and stress distribution along the cross section.

2.2.3 Elastic properties of silicon

Silicon has a diamond structured lattice and the $\{111\}$, $\{100\}$ and $\{110\}$ Miller indices are the most important. The $\{100\}$ and $\{110\}$ planes intersect at 45 degrees, while the $\{111\}$ and $\{100\}$ planes intersect at 54.7 degrees. Unlike isotropic materials whose elastic properties are independent of orientation and are characterised by a single elastic constant, the elastic properties of crystals usually dependent on the orientation with respect to a reference axis. The relation of the crystallographic orientation with the elastic constant E for $\{100\}$ oriented silicon is shown in figure A.1, appendix A.

2.2.4 The piezoresistive effect in silicon

Although the piezoresistive effect in polycrystalline and crystalline materials has been known since the 1930s, C.S.Smith was the first researcher to investigate this effect in silicon in 1954. The piezoresistive effect in silicon is due to the stress induced deformation of the silicon energy bands. When a piezoresistor is electrically powered, it is said to operate in longitudinal mode when the stress/strain and electrical current have parallel orientation. When the stress and the electrical current are orientated perpendicularly the piezoresistor is said to operate in transverse

mode, as shown in figure 2.6.

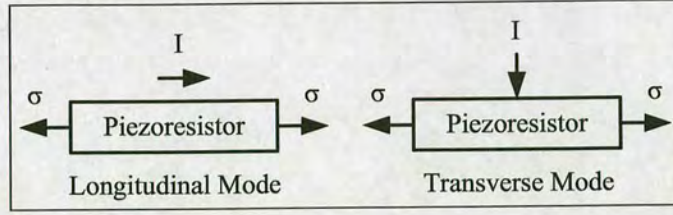


Figure 2.6: *Piezoresistor modes.*

In the case of doped silicon, the models that are used to interpret the piezoresistive effect depend on the type of dopant (ie whether the material is p-type or n-type doped) [22, 23]. The piezoresistance is quantified by the piezoresistance coefficients described by equation 2.7.

$$\Pi_{xx} = \frac{1}{\sigma} \frac{\Delta\rho}{\rho} \quad (2.7)$$

where $_{xx}$ is the coefficient parameter, σ is the applied stress and ρ is the semiconductor resistivity. Obviously, the change in the piezoresistive coefficients is linearly related to the induced stress. The piezoresistance components for intrinsically p-type and n-type silicon at room temperature have been derived experimentally by Smith and are listed in table 2.1.

Type	Resistivity	Π_{11}	Π_{12}	Π_{44}	$\frac{1}{2}(\Pi_{11} + \Pi_{12} + \Pi_{44})$	$\frac{1}{2}(\Pi_{11} - \Pi_{12} - \Pi_{44})$
Units	$\Omega \cdot cm$	$10^{-11} Pa^{-1}$	$10^{-11} Pa^{-1}$	$10^{-11} Pa^{-1}$	$10^{-11} Pa^{-1}$	$10^{-11} Pa^{-1}$
p-type	7.8	6.6	-1.1	138.1	71.8	-66.3
n-type	11.7	-102.2	53.4	-13.6	-31.2	-17.6
Crystallographic Orientation	-	{100}	{100}	-	{110}	{110}
Piezoresistor Mode (Longitudinal / Transverse)	-	Lon.	Trans.	-	Lon.	Trans.

Table 2.1: *Piezoresistive coefficients for single crystalline intrinsically doped silicon derived by Smith [24].*

The strain gauge sensitivity may also be quantified through the gauge factor K defined in equation 2.8.

$$K = \frac{1}{\epsilon} \frac{\Delta\rho}{\rho} = E \frac{1}{\sigma} \frac{\Delta\rho}{\rho} = E_{[ccc]} \Pi_{xx} \quad (2.8)$$

where ϵ is the resultant strain, $E_{[ccc]}$ is silicon crystallographic orientation dependent Young's modulus and Π_{xx} is the corresponding piezoresistive coefficient. Combining the piezoresistive coefficient values from table 2.1, equation 2.8 and Young's modulus values for silicon from figure A.1 in appendix A, the gauge factors for intrinsically doped single crystalline silicon are derived and are listed in table 2.2.

Type	Resistivity ($\Omega \cdot cm$)	Gauge factors			
p-type	7.8	8.59	-1.43	121	-112
n-type	11.7	-133	69.5	-52.7	-29.7
Young's Modulus (GPa)	-	130.2	130.2	168.9	168.9
Crystallographic Orientation	-	{100}	{100}	{110}	{110}
Piezoresistor Mode (Longitudinal / Transverse)	-	Lon.	Trans.	Lon.	Trans.

Table 2.2: Gauge factors for doped single crystalline silicon derived using piezoresistive coefficients by Smith [24].

The transformation of the components to the polar system has been carried out by Yozo Kanda [25] and the variation of n-type and p-type crystalline silicon piezoresistive coefficients according to the silicon crystallographic orientation on the {100} plane are shown in figure A.4, appendix A. Although n-type piezoresistors operating in longitudinal mode along the {100} crystallographic orientation are marginally more sensitive than the corresponding p-type piezoresistors, n-type silicon does not possess longitudinal and transverse symmetric sensitivity properties. A useful property of p-type silicon is that the transverse and longitudinal coefficients along the {110} crystallographic axes have opposite sign while the magnitude is almost equal, as can be seen in tables 2.1, 2.2 and figure A.4b, appendix A. This property renders p-type crystalline silicon piezoresistors an attractive solution for the fabrication of full-active Wheatstone bridge circuits with four p-type piezoresistors. Due to the symmetry of p-type piezoresistive coefficients in longitudinal and transverse mode, the full-active Wheatstone bridge differential output voltage would be approximately linear.

Kanda has also calculated the relative variations of piezoresistive factors for p-type monocrystalline silicon with respect to temperature, reprinted in figure A.3 in appendix A [25]. It is observed that maintaining a strain gauge doping concentration lower than $10^{18} atoms/cm^2$ should not compromise the sensitivity of the piezoresistive sensitivity due to temperature variations.

However, the author has noted that the values shown in the diagram deviate from published experimental values for doping concentrations higher than $5 \times 10^{18} \text{ atoms/cm}^2$ implying that the theoretical models used to calculate temperature induced variations in piezoresistive coefficients maybe inaccurate.

Kleinmann *et al.* has published transverse and longitudinal transverse gauge factors for single crystalline silicon with respect to dopant concentration. This relationship can be seen in figure A.2, appendix A [23] and it is obvious that to gain maximum strain gauge sensitivity the dopant concentration should be kept at minimum.

Sandmaier and Küll have fabricated p-type piezoresistive strain gauges for application in pressure sensors using boron ion implantation with activation at 1000°C for 65 minutes [26]. The authors have derived experimentally the gauge factor along the $\{110\}$ silicon plane, which has been approximately 86 in longitudinal and transverse piezoresistive modes.

Literature review in this section has shown that due to symmetry properties, use of p-type silicon piezoresistors oriented along the $\{110\}$ silicon crystal planes often are the best approach for the fabrication of full-active Wheatstone bridge circuits. Optimal piezoresistive sensitivity is achieved for low dopant concentrations. Low dopant concentration also offers reduced temperature induced variations in the piezoresistive coefficients, which is desirable.

2.2.5 Maximization of strain gauge sensitivity with stress concentration regions

Generally MEM systems with integrated strain gauges aim to maximize the stress in the area of the gauges in order to optimize the device sensitivity. As mentioned previously, equations 2.7 and 2.8 show that the change in piezoresistivity $\frac{\Delta\rho}{\rho}$ is proportional to the applied stress and strain respectively. In this project, single crystalline silicon strain gauges are integrated with silicon cantilever beams and their sensitivity performance should be optimized. This is achieved with the introduction of stress concentration regions (SCR) that are usually sharp structural changes in the region of the fabricated piezoresistors. R. Bashir *et al.* have shown that by reducing locally the thickness of a cantilever beam, a 61% increase in the piezoresistive sensitivity could be achieved [27]. To maintain a relatively simple micromachining process, a different approach has been chosen here and planar stress concentration regions next to the fixed end of the cantilevers are investigated. For an axially stressed beam of non-uniform cross section, illustrated in figure 2.7, the stress concentration factor SCF is defined as

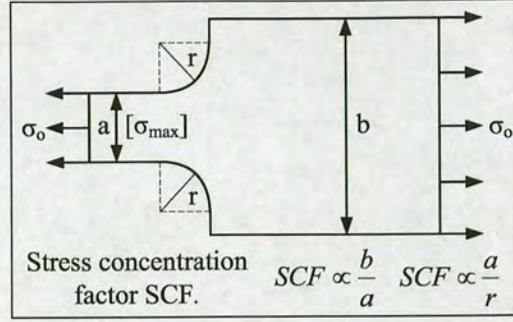


Figure 2.7: Axially stressed beam of non-uniform cross section.

$\sigma_{max} = SCF \times \sigma_o$. SCF is proportional to ratios b/a and a/r , where r is the radius of the fillets [28].

2.2.6 ANSYS finite element simulations

To investigate the effect of structural variations of planar stress concentration regions in cantilevers that are mechanically deformed in pure bending mode, ANSYS finite element modeling simulations has been carried out. The finite element model, which represents the proposed MEM wind sensing system, has been generated using SOLID95 elements and is shown in figure 2.8. Higher element density in the stress concentration region improves the modeling accuracy.

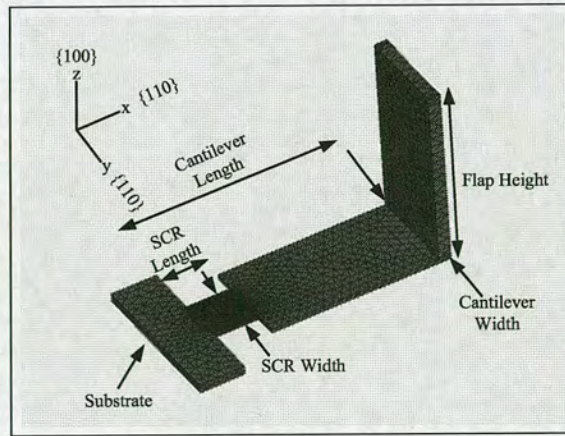


Figure 2.8: ANSYS finite element model of the proposed MEM cantilever-flap system.

The width of the cantilever has been kept constant at $300\mu m$. The dimensions of the vertical flap have been kept constant at $600\mu m$ height, $300\mu m$ width, and $40\mu m$ thickness. $10KPa$ pressure has been applied to the flap and the stress in the concentration region has been recorded. Simulations have shown that variation in the cantilever and stress concentration lengths did not

impact on the resultant stress. The dependance of the simulated resultant stress to the thickness of the cantilever and the width of the concentration region is shown in figure 2.9.

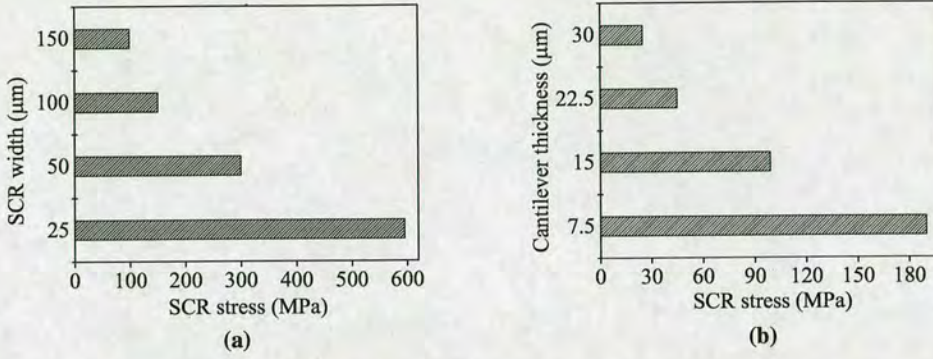


Figure 2.9: Simulated axial stress in the stress concentration region as function of a) stress concentration region width, and b) cantilever thickness and stress concentration width thickness.

In the simulations performed here only the stress on the surface of the cantilever beams has been recorded, while piezoresistors that are introduced in silicon through implantation have a finite depth, implying that the average stress they detect differs from the simulated values. When the MEM devices are fabricated, at least one SiO_2 passivation layer is deposited on the substrate to provide electrical insulation between the metallisation and the substrate. This results in a composite silicon-silicon oxide beam that has different mechanical characteristics to the simulated structure. Furthermore, additional layers added on the silicon surface imply that piezoresistors are buried beneath the cantilever beam surface and are located closer to the neutral axis, hence are exposed to smaller amounts of stress/strain, as can be seen in figure 2.5. As mentioned previously, the stress concentration factor is inversely proportional to the fillet radius r . For the simulations 90° degree sharp feature corners have been used, which is not realistic because light diffraction effects during the photolithographic exposure cause features to have rounded corners. Therefore, the fillet radii of the features at the stress concentration region cannot be known prior to the fabrication of the devices, hence the effect of rounded corners cannot be taken into account during the simulations.

Fabrication parameters such as the average stress along the boron implanted piezoresistors having finite depth in the silicon cantilever beams, the thickness of the SiO_2 dielectric deposited on the cantilever surface, as well as the radii of feature corners are not known beforehand. Furthermore, estimation of the resultant drag across the flaps using fluid dynamics equations is very

complex, as discussed in subsection 2.2.1. For these reasons, the anticipated stress results on the stress concentration region of cantilever beams derived from ANSYS simulations are likely to have discrepancies between simulated and actual experimental results.

Nevertheless, the benefit of performing simulations has been to gain insight into the geometrical design parameters and the design trends that would lead to optimization of the device sensitivity. The main conclusion to be drawn from the simulations is that when a cantilever beam-with a planar stress concentration region-is in pure bending, reducing the cantilever thickness and increasing the ratio b/a (shown in figure 2.9) result in increased stress in the concentration region and therefore in increased piezoresistive sensitivity.

2.2.7 Wheatstone bridge circuit

The Wheatstone bridge is a very popular circuit for implementation with strain gauges. The use of four adjacent resistors occupying a small area implies that temperature variations affect all resistors equally, without affecting the output offset voltage of the bridge. Table 2.3 lists the possible configurations and output voltages in a Wheatstone bridge.

Configuration	a	b	c	d
Output voltage	$\frac{V_{in}}{4} \frac{\Delta R}{(R + \frac{\Delta R}{2})}$	$\frac{V_{in}}{2} \frac{\Delta R}{(R + \frac{\Delta R}{2})}$	$\frac{V_{in}}{2} \frac{\Delta R}{R}$	$V_{in} \frac{\Delta R}{R}$
Normalized output	0.235	0.47	0.5	1

Table 2.3: Wheatstone bridge circuit configurations with a) one, b,c) two and d) four active arms. Upward (downward) arrow direction indicates an increase (decrease) in the resistance of the arm.

A full-active, p-type, boron doped Wheatstone bridge circuit realized in a single crystalline n-type silicon substrate is shown in figure 2.10. In figure 2.10a is shown a perfectly balanced Wheatstone bridge aligned to the $\{110\}$ crystallographic axes of the silicon substrate. Due to the absence of stress, the four arms of the bridge circuit ($R1$, $R2$, $R3$ and $R4$) have equal resistance values, and the differential output signal ΔV is 0 ($V_1 = V_2 \Leftrightarrow \Delta V = 0$). If a stress σ is applied, as shown in figure 2.10b, the resistance of the four arms will be modified due to

the piezoresistive effect described earlier in section 2.2.4.

Resistors $R1$ and $R3$ are operating in transverse mode and the reduction in their resistance is $\Delta R = R \times \frac{1}{2}(\Pi_{11} + \Pi_{12} - \Pi_{44}) \times \sigma$, where R is the initial resistance, Π_{xx} is the corresponding piezoresistive component and σ is the applied stress. Resistors $R2$ and $R4$ are operating in longitudinal mode and the increase in their resistance is $\Delta R = R \times \frac{1}{2}(\Pi_{11} + \Pi_{12} + \Pi_{44}) \times \sigma$. These changes in the resistance of the four arms of the bridge circuit result in a differential voltage $\Delta V = V_1 - V_2$.

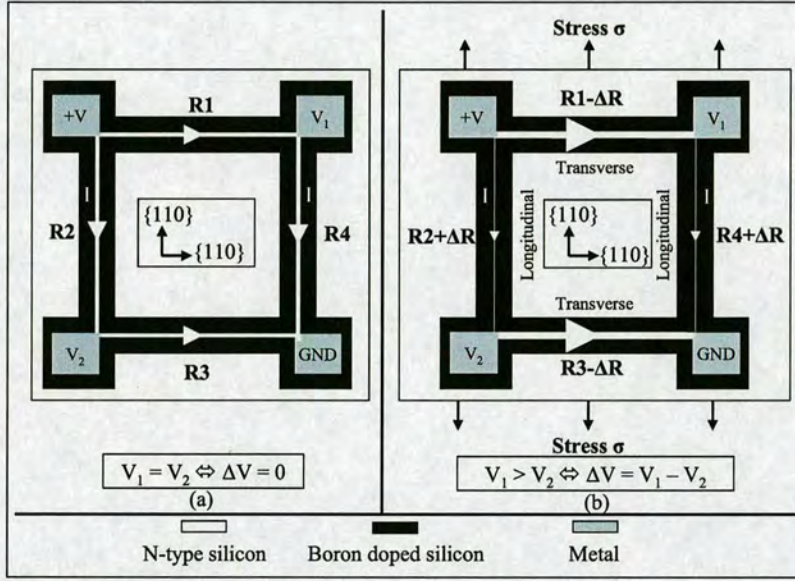


Figure 2.10: Realization of a p-type Wheatstone bridge circuit in n-type single crystalline silicon substrate: a) without stress, b) with applied stress.

Full Wheatstone bridge circuits with four variable resistors are widely used in pressure sensors, where the electrical circuit layout is straightforward. However, to our knowledge, apart from applications in atomic force microscope where only one or two cantilevers are used at a time [29], the full-active Wheatstone bridge circuit is not found in the literature to be integrated with cantilever beams in larger scale (32 bridges per die or more) for integration with LSI circuits on robots due to challenges in the circuit layout and device design. In this project, design (d) with four active arms has been implemented in chapter 4 and design (b) with two active arms has been implemented in chapter 5.

2.2.8 Frequency response of the proposed MEM system and comparison with literature data

A cantilever beam resonates when it is excited in one of its principal modes of vibration. In resonance all moving parts of the system are oscillating in phase with one frequency [30]. The resonant frequency f of the fundamental mode of vibration of a uniform cantilever beam is given by equation 2.9 [31].

$$f = \frac{1.875^2}{2\pi} \sqrt{\frac{EI}{\rho AL^4}} \quad (2.9)$$

where E is the Young's modulus, ρ is the density of the material, A is the cross sectional area of the beam and L is the length of the structure [31]. I expresses the flexural rigidity of the cantilever beam structure and is defined by equation 2.10.

$$I = \frac{w \cdot t^3}{12} \quad (2.10)$$

where w and t is width and the thickness of the cantilever respectively.

Here, the proposed MEM systems consist of cantilevers of non-uniform area with a flap at their free end, which effectively acts as an added mass at the tip of the cantilevers. Although the formula 2.9 used for the calculation of the resonance frequency of the cantilever beams will yield only approximate numerical results in our case, it is useful in obtaining an estimation of the natural response of the proposed system. For a silicon cantilever beam of constant cross section with $600\mu\text{m}$ length, $300\mu\text{m}$ width and $15\mu\text{m}$ thickness, the fundamental resonant frequency has been calculated using equation 2.9 to be 587KHz . If the cantilever beam's length is increased to $1500\mu\text{m}$, its calculated resonant frequency is reduced to 90.8KHz .

Resonance frequencies of the cantilever-flap systems are indicated in figure 2.11, points (c) and (d). It can be seen that the MEM cantilever-flap systems have very different frequency response characteristics compared to the cricket's mechanoreceptors (curves (a) and (b)). The cantilever-flap systems have a very narrow frequency bandwidth in comparison to the cricket's mechanoreceptors. Furthermore, the proposed MEM systems exhibit resonance at much higher frequencies than the cricket's mechanoreceptors. The above imply that the proposed MEM systems would not be perfectly adapted to the cricket's environment. Although the proposed MEM artificial hair cells will not possess a frequency response similar to that of the wind mechanoreceptors of the cricket, the design was thought to be sufficient for studying the evasive

behavior of the cricket in response to wind motion caused by predatory action.

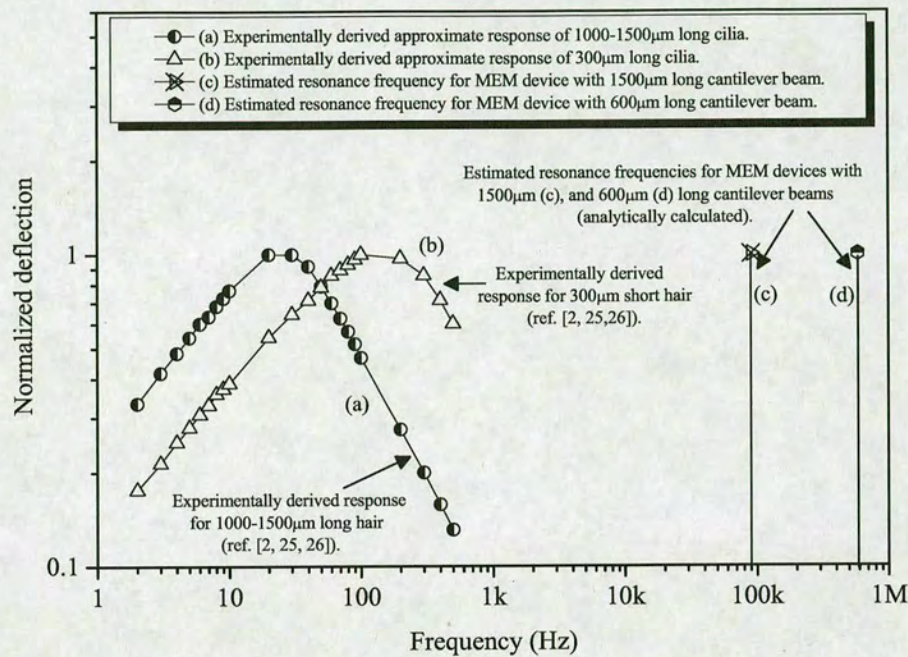


Figure 2.11: *a, b) experimentally derived frequency response of cricket's wind mechanoreceptors, c, d) analytically estimated frequency response of the proposed MEM artificial hair cells.*

2.3 Device specification

The project involves the fabrication of cantilever beams with flaps at their free ends, with lengths ranging from $400\mu\text{m}$ to $1100\mu\text{m}$. Each cantilever is to be integrated with a piezoresistive Wheatstone bridge circuit. The Wheatstone bridge will be powered by a $+3.3\text{V}$ power supply and the bridge resistance should be as high as possible to reduce the electrical current and the power consumption. The Wheatstone bridge circuit should have linear current-voltage characteristics and will be interfaced to a large scale integration (LSI) neuron circuit that produces electrical spikes when change in the differential output of the Wheatstone bridge is detected. The minimum differential output voltage of the device should be 0.3mV at 0.1m/s wind speed and the operational wind speed of the MEM sensor would range between 0.1m/s and 3.9m/s . Metal oxide semiconductor field effect transistor (MOSFETs) amplifiers may be designed and integrated on the same substrate with the wind sensor to provide a boost to the differential output signal of the Wheatstone bridge circuit. It has been decided that thirty two wind sensing elements should be fabricated in each die, which requires a high yield microfabrication process. The die area of the MEM sensor should be approximately 1cm^2 . An overview of the MEM system including the Wheatstone bridge circuit, the neuron LSI integrated circuit and the robot is shown in figure 2.12.

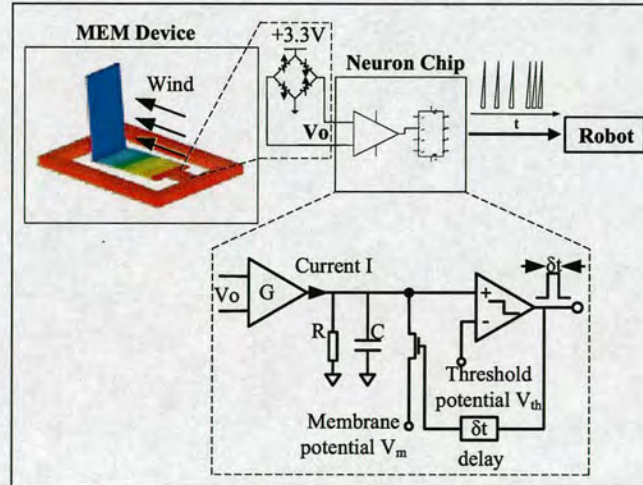


Figure 2.12: Overview of the MEM air flow sensor, the neuron LSI circuit and the robot.

The differential output of the Wheatstone bridge that is integrated with the cantilever-flap system is detected by the operational amplifier with gain G that produces a current I and charges the RC circuit exponentially. When the electrical potential across the capacitor reaches the

threshold potential V_{th} , the comparator produces an electrical spike V_o with duration δt , and the capacitor C is discharged after short delay δt and acquires the membrane potential V_m . This process continues as long as the operational amplifier detects a differential output voltage from the Wheatstone bridge. The electrical spikes produced by the neuron circuit are transmitted to the robot, which processes the spikes and uses algorithms to control its behavior.

2.4 Conclusion

The models that describe the cricket's wind mechanoreceptors and the hair-air system have been presented in section 2.1. Literature research has shown that the cricket's wind mechanoreceptors act as band pass filters in the ~ 0 -1 KHz frequency range and the frequency selectivity of the hairs is classified according to their length. Long hairs are more sensitive to low frequency and short hairs are more sensitive to high frequency particle oscillation, as has been shown in figure 2.11, curves (a) and (b). This is the reason why long hairs are termed 'velocity' and short hairs are termed 'acceleration' sensitive.

Although an attempt has been made to simulate -by analytical fluidic computations in section 2.2.1- the drag caused by air motion to the out of plane flaps, the system is very complex and it would not have been possible to obtain realistic numerical results. It has been shown in section 2.2.4 that, due to the piezoresistive symmetric properties of p-type silicon along the $\{110\}$ crystallographic plane, p-type piezoresistors are the best option for use in full-active Wheatstone bridge circuits. In section 2.2.6 ANSYS simulations have been performed and have shown that to optimize the sensitivity of the strain gauges, the cantilever thickness and the width in the stress concentration region have to be minimized.

Comparison of the frequency response between wind mechanoreceptors of the cricket and analytically calculated frequency response of the proposed MEM wind sensor is illustrated in section 2.2.8, figure 2.11, and verifies that the MEM devices with the given specification will not achieve characteristics that mimic the frequency response of the cricket's wind mechanoreceptors. Nevertheless, these issues had not been anticipated by our collaborator Dr. Barbara Webb at the time of the device design stage and therefore it had been decided to pursue the proposed cantilever beam - out of plane flap MEM system.

As aforementioned, the proposed MEM system consists of: a) Wheatstone bridge circuits made of a patterned metallisation and p-type boron doped microfeatures implanted in n-type single

crystalline silicon, b) silicon cantilever beams that are integrated with the full-active Wheatstone bridge circuits, and c) out of plane flaps that are integrated at the free end of silicon cantilever beams. The development of boron p-type full-active Wheatstone bridge circuits, integrated with metallisation is described next in chapter 3.

Chapter 3

Characterisation of boron implantation and fabrication of test circuits

As discussed in chapter 2, the proposed MEM system consists of: a) Wheatstone bridge circuits made of a patterned metallisation and p-type boron doped microfeatures implanted in n-type single crystalline silicon, b) silicon cantilever beams that are integrated with the full-active Wheatstone bridge circuits, and c) out of plane flaps that are integrated at the free end of silicon cantilever beams.

The development of Wheatstone bridge circuits consisting of p-type boron doped microfeatures and metallic electrodes is described in this chapter. For the convenience of the reader, a summary of the fabrication process is illustrated in figure 3.8, page 40. Here the circuits are fabricated by selective implantation of n-type crystalline silicon substrate with p-type boron, forming a p-n junction. Selective implantation of a n-type silicon substrate is achieved by deposition of a SiO_2 mask on the substrate surface, which is photolithographically patterned to define the desired microfeatures. Next the SiO_2 mask is selectively removed by a dry etch step to reveal the underlying crystalline n-type silicon, which is heavily implanted with p-type boron. After implantation, the boron impurities are electrically activated by a high temperature anneal step. Next the implanted regions are passivated with SiO_2 to prepare the p-type features for integration with a metallisation. Contact windows are patterned photolithographically and the SiO_2 passivation is etched, revealing selectively the p-type boron microfeatures. Finally the metallisation layer is deposited on the substrate and contacts the p-type boron doped microfeatures through the predefined contact windows. Subsequently the metallisation is photolithographically patterned and etched selectively to define the desired electrodes, completing the fabrication of metallisation – p-type silicon Wheatstone bridge circuits. The circuits can be electrically probed to obtain the Wheatstone bridge resistance and offset voltage.

This chapter begins with the characterisation of boron implantation into blank silicon wafers by TSuprem4 simulations, secondary ion mass spectroscopy (SIMS) and electrical 4-point sheet

resistance electrical measurements in section 3.1. In section 3.2 the photolithographic mask designs are presented; the designs are used for: a) the selective implantation of p-type boron microfeatures in n-type silicon substrate, b) the definition of metal – semiconductor contact windows and c) the definition of metallic electrodes.

Using the designed photolithographic masks, the lithographic process is developed in section 3.3, followed by the fabrication of boron doped microfeatures integrated with two different metallisations (titanium nitride/titanium and aluminium 1 percent silicon) in section 3.3. Finally, the electrical properties of fabricated Wheatstone bridge circuits are presented in section 3.4.3.

3.1 Boron implantation characterisation

Boron doping of blank, n-type silicon substrates was performed by implantation at Ion Beam Services. For the chosen impurity the available implantation doses ranged from 10^{11} atoms/cm² to 10^{17} atoms/cm² and the ion acceleration energies ranged from 30keV to 160keV.

Initially 3-inch wafers were used for the purpose of process development. The wafers have {100} crystal orientation and the average substrate resistivity has been measured in an automatic 4-point probe station to be $2\Omega\cdot\text{cm}$. Thin PECVD SiO₂ layers of 100nm, 150nm and 200nm thicknesses have been deposited on some wafers in order to examine the distribution of boron implanted in silicon through SiO₂ and the simulation accuracy for boron implantation through thin oxide films. The aforementioned SiO₂ layers would be removed after implantation by wet etching in a buffered hydrofluoric acid solution. Subsequently the boron would be activated and the dopant profile would be characterised using ion mass spectroscopy and 4-point sheet resistance measurements.

The wafers have been implanted with boron using 3.5×10^{13} atoms/cm² dose, 30keV, 55keV, and 80keV energies, and 0 degree tilt and rotation. For implantation doses ranging between 10^{14} atoms/cm² and 10^{15} atoms/cm² at 70keV implantation energy, a 35 minute annealing process at temperatures higher than 900°C, have shown to fully activate the implanted boron impurities [32]. Here, the implanted wafers have been annealed at 1000°C for 35 minutes in N₂ atmosphere to activate the boron.

In the next sections the implanted and activated boron is characterised by three techniques: a) secondary ion mass spectroscopy which yields the impurity distribution profile along the

depth of the implanted substrate, b) TSUPREM-4 simulations that yield the implanted impurity distribution profile and sheet resistance, and c) experimental sheet resistance extraction with 4-point automatic probing.

3.1.1 Secondary ion mass spectroscopy

Distribution curves of the implanted and activated boron have been obtained with secondary ion mass spectroscopy using an O^+ sputter beam. The boron profile for implantation in blank silicon can be seen in figure 3.1a.

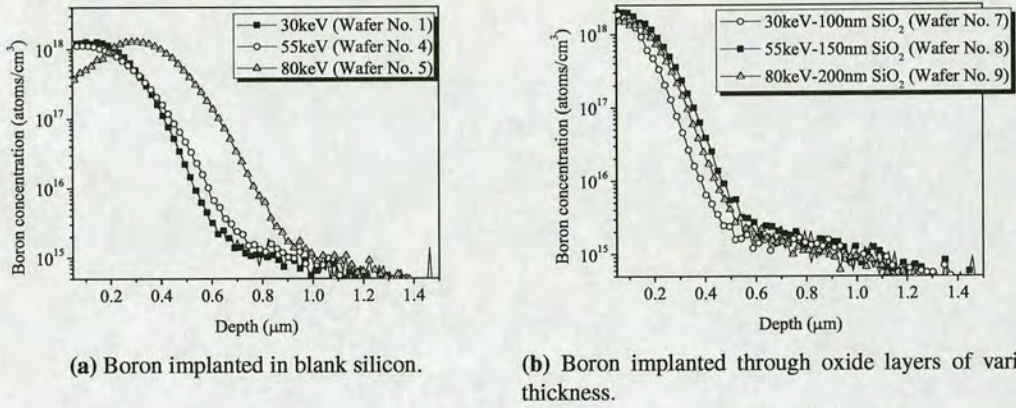


Figure 3.1: Boron distribution profiles obtained by the SIMS method for various implantation energies. The implantation dose has been 3.5×10^{13} atoms/cm² and activation has been performed at 1000°C for 35 minutes in N₂ environment.

It is observed that, for implantation in blank silicon, the main effect of increasing the energy from 30keV to 55keV is the slightly broadened body tail of the distribution curve. Further increase of the implantation energy to 80keV results in a shift of the distribution curve towards the right. The distribution profile for all energies flattens at larger depths due to ionic boron channeling effects through the crystalline silicon lattice.

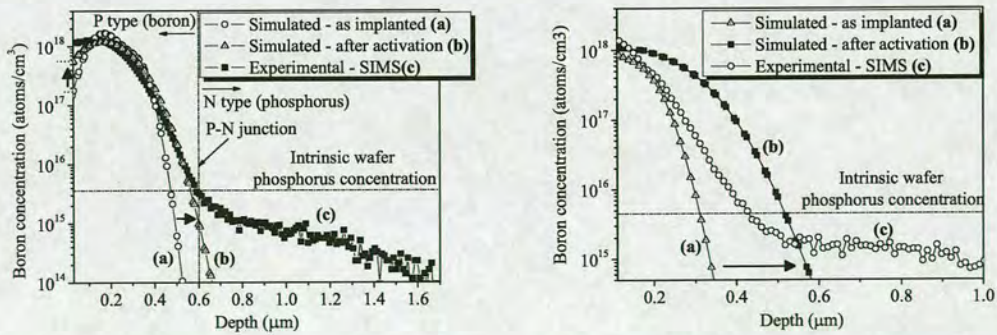
In figure 3.1b the distribution profile of boron implanted in silicon through thin SiO₂ layers of variable thickness can be seen. An added thin SiO₂ layer above the implanted silicon regions absorbs partly an ion's energy and randomizes its direction. These effects cause a shallower boron distribution compared to implantation in blank silicon. Here, for implantation in silicon through thin SiO₂ layers, both the SiO₂ thickness and the implantation energy have been increased simultaneously, as can be seen in the legend box in figure 3.1b. The increas-

ing SiO₂ layer thickness from 100nm to 150nm to 200nm effectively canceled the increase in implantation energy from 30keV to 55keV to 80keV leading to similar boron distribution profiles for all energies. This can be clearly seen in the figure, where all distribution profiles are similar. Furthermore, the distribution profiles for implantation in silicon through SiO₂ are shallower compared to profiles obtained for boron implantation into blank silicon. Simulations with TSuprem4 software have been performed next.

3.1.2 TSuprem4 simulations

TSuprem4 is a simulation software that models the distribution profile of implanted impurities and extracts the sheet resistance of the implanted regions. Researchers at the University of Texas at Austin have shown in a series of publications that the concentration distribution profile of implanted boron can be successfully modeled with the Dual Pearson model [33–35]. The model that has been developed by these researchers has been incorporated into TSuprem4 and allows the simulation of boron implantation for energies between 30keV and 80keV, with doses between 10^{13} atoms/cm² and 10^{16} atoms/cm², and variable tilt and rotation angles.

Shown in figure 3.2a, curve (a), is a selected simulated boron distribution profile for implantation in blank silicon with 30keV acceleration energy and 3.5×10^{13} atoms/cm² dose. In figure 3.2b, curve (a), is shown a selected simulated boron distribution profile for implantation in silicon through SiO₂, prior to the boron activation.



(a) Boron implanted in blank silicon (wafer No.1).

(b) Boron implanted in silicon through 100nm thick SiO₂ layer (wafer No. 7).

Figure 3.2: Comparison of simulated and experimentally (SIMS) obtained boron distribution profiles. Implantation energy: 30keV, implantation dose: 3.5×10^{13} atoms/cm².

During the high temperature anneal process that serves to activate the boron atoms, solid state

diffusion occurs and the boron is redistributed. This process has been studied by Hofker *et al.* who found that the concentration near the surface increases and the tail broadens [36]. This trend is also observed here, in figures 3.2a and 3.2b between curves (a) and (b), as indicated by the dark arrows. The boron concentration profiles are observed to broaden after the simulated implantation and activation.

For implantation in blank silicon, the experimentally obtained data from SIMS and the simulated data from TSuprem4 are in good agreement, as can be seen in figure 3.2a, curves (b) and (c). For implantation in silicon through a thin SiO₂ layer, the simulation results seen in figure 3.2b, curve (b), do not match well with the experimentally (curve (c)) obtained results. From observation of the distribution curves, this discrepancy is likely to be due to the fact that simulations do not consider the randomization effect of the SiO₂ layer, but take into account only its ion stop properties. It can also be seen in both figures 3.2a and 3.2b that TSuprem4 simulations do not take into account the channeling effects that occur at larger depths due to the silicon crystallographic properties, since the simulated boron distribution profiles (curves (a) and (b)) do not flatten as in the experimentally obtained profiles (curves (c)) in both subfigures 3.2a and 3.2b. The sheet resistances of boron implanted areas have been extracted through simulations and are compared with experimental measurements which are performed in 4-point automatic probe station.

3.1.3 4-point sheet resistance electrical measurements of boron implanted wafers

The sheet resistance of implanted boron has been extracted with 4-point probe measurements. It has been found that additional cleaning of sample surfaces in fuming nitric acid followed by a clean in a buffered hydrofluoric acid solution, after the implantation and high temperature activation (1000°C / 35 minutes / N₂ environment) of the impurities, reduced the standard deviation of the 4-point measurements. Comparison of the experimentally derived and TSuprem4 simulated sheet resistances can be seen in figure 3.3, where the vertical error bars indicate the standard deviation across the electrical measurements. It is observed in graph 3.3 that simulated sheet resistance values are consistently higher than experimentally obtained resistance values.

Given the excellent agreement between the simulated and experimentally obtained boron distribution profiles (fig.3.2a, curves (b) and (c)), the aforementioned mismatch in the sheet resistances (shown in fig.3.3) implies that the boron activation has been incomplete. Therefore, the concentration of activated boron is actually slightly lower than shown in figure 3.1a. As can

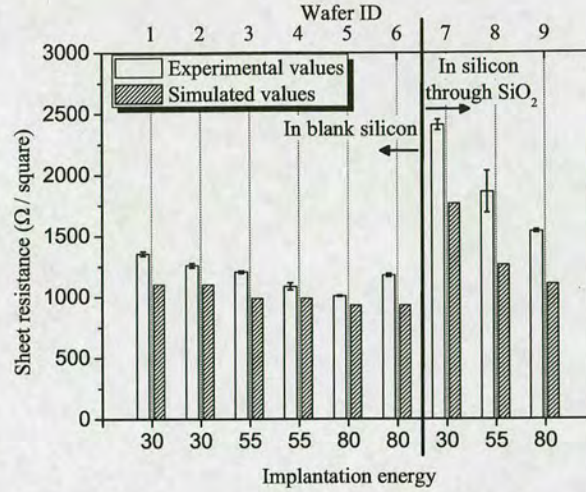


Figure 3.3: Simulated and experimentally obtained (SIMS) sheet resistance values for implanted (variable acceleration energies - 3.5×10^{13} atoms/cm² dose) and activated boron.

be seen in the same figure, the maximum boron concentration for all implantation acceleration energies (30keV, 55keV, 80keV) is less than 1×10^{18} atoms/cm³. This is desirable because at these concentration levels the temperature induced variations in the piezoresistive coefficients is minimized, as can be seen in figure A.3, appendix A.

Next in section 3.2 the photolithographic masks designed to fabricate metal – p-type silicon circuits are presented.

3.2 Design of photolithographic masks

Figure 3.4 illustrates the design of test structures used in this phase of the project. The test structures included in this mask design are: i) metallic Greek crosses for measuring the electrical properties of the fabricated metallisation, ii) Kelvin resistors for the characterisation of metal – p-type boron doped silicon interfacial contacts, and iii) serpentine shaped Wheatstone bridge test circuits with metal – semiconductor contact windows and patterned metallisation for electrical probing. Fabrication of these structures requires three photolithographic layers: a) the first layer defines the implantation mask windows, b) the second layer defines the metallisation – p-type silicon contact windows, and c) the third layer defines the metallic electrodes' shape.

To determine the metallisation resistance a Greek Cross test structure is probed by applying

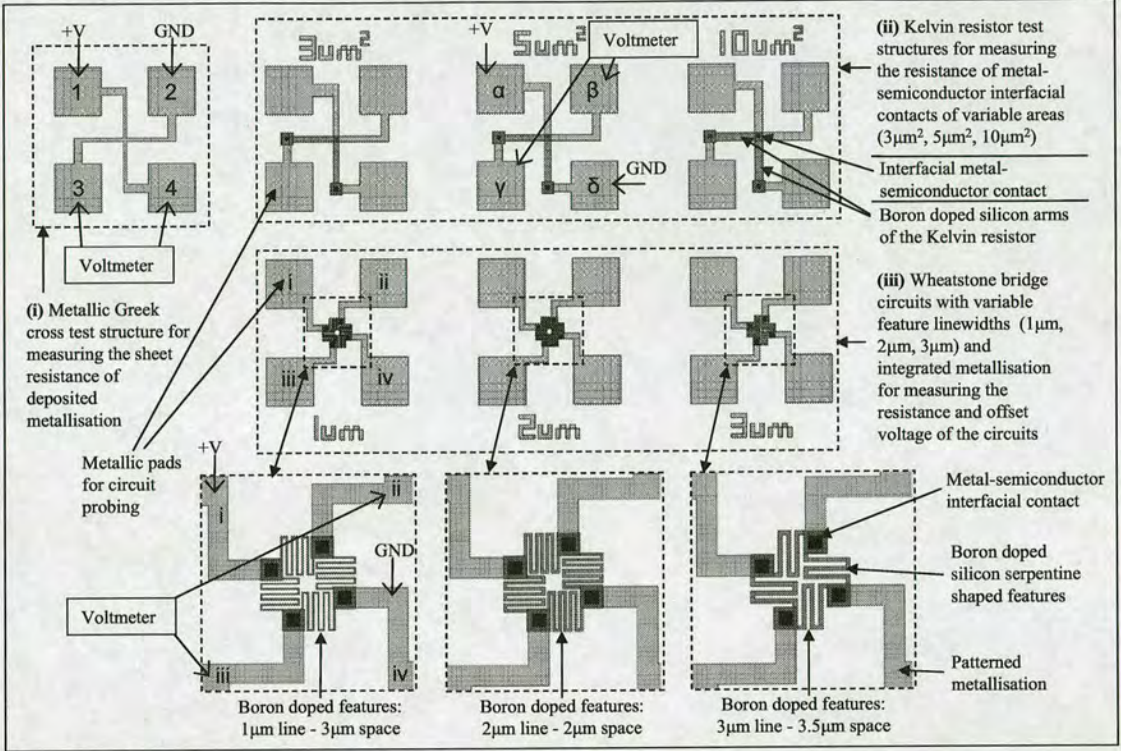


Figure 3.4: A Greek cross, Kelvin resistors and Wheatstone bridge test circuits used for the characterisation of the photolithographic process, the boron implantation and its integration with a metallisation.

electrical current I_{12} through pads 1-2 and by measuring the voltage V_{34} between pads 3-4. The sheet resistance R_s can be calculated using equation 3.1 [37].

$$R_s = \frac{\pi}{\ln 2} \frac{V_{34}}{I_{12}} \quad (3.1)$$

The thin film resistivity can be derived using equation $\rho = R_s t$, where R_s is the measured sheet resistance and t is the thickness of the film.

To determine the metal – semiconductor interfacial contact resistance, a Kelvin resistor is probed by applying electrical current $I_{\alpha\delta}$ through pads $\alpha - \delta$. The current flows from the metallic arm α into the metal – semiconductor interfacial contact and into the boron doped arm, ending to the metallic pad δ . The voltage drop $V_{\beta\gamma}$ across the interfacial contact is measured by probing pads $\beta - \gamma$. The interfacial contact resistance R_c can be calculated using equation 3.2 [38, 39].

$$R_c = \frac{V_{\beta\gamma}}{I_{\alpha\delta}} \quad (3.2)$$

The specific resistivity ρ_c of the metal – semiconductor interfacial contact can be derived using the equation $\rho_c = R_c A$, where A is the area of the contact [38].

Finally, the electrical characterisation of Wheatstone bridge circuits includes measurements of their resistance and offset voltage. To measure the electrical resistance of a bridge, a voltage is applied across two opposite nodes (i) and (ii), and the resultant current is recorded. At the same time the bridge offset voltage can be measured with a voltmeter across the two remaining opposite nodes (iii) and (iv).

The fabrication of test circuits shown in figure 3.4 is described in the next sections, starting with the development of the photolithographic process in section 3.3.

3.3 Characterisation of the photolithographic process

To fabricate the test structures described in the previous section a 4-inch mask with three $1 \times 1 \text{ cm}^2$ fields has been designed here and has been manufactured commercially. The three fields are used for: i) the definition of the boron doped serpentine shaped Wheatstone bridges and the boron doped arms of Kelvin resistors, ii) patterning the metal – p-type semiconductor contact windows, and iii) patterning the metallisation. To develop the photolithographic process, silicon wafers have been diced to 1 cm^2 pieces, to be patterned in a Cobilt mask aligner using an i-line (365nm) ultraviolet light source. Figure 3.5 shows how the samples have been attached on a carrier wafer using sticky tape to perform the photolithographic process.

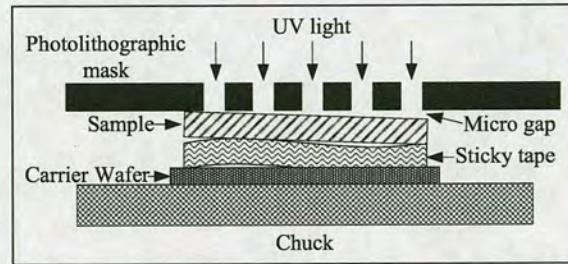


Figure 3.5: Setup of the photolithographic process with shards in the Cobilt.

Figure 3.6, illustrates an exposed and developed sample where the feature on the right has been exposed properly in contrast to the feature on the left. The theoretical minimum linewidth resolution for contact lithography is given by the formula $2 \times b_{min} = 3 \times \sqrt{\lambda \times (g + \frac{\delta}{2})}$, where b_{min} is the minimum linewidth, λ is the exposure wavelength, g is the gap thickness between the sample and the photolithographic mask, and δ is the photoresist thickness [40]. The min-



Figure 3.6: *Optical micrograph of incorrectly (left) and correctly (right) exposed adjacent features.*

imum linewidth for the process here is $b_{min} = 0.73\mu\text{m}$, assuming no spacing between the photolithographic mask and the substrate ($g = 0$), and having a measured photoresist thickness of $\delta = 1.3\mu\text{m}$. This value being smaller than the $2\mu\text{m}$ linewidth features printed here, forces the conclusion that the incorrect exposure observed is due to near field Fresnel diffraction, which arises when a finite distance separates the aperture and the surface where the UV radiation is projected [41]. Here gap(s) between the photolithographic mask and the sample exist for two possible reasons: a) the quartz mask does not maintain its flatness because non-uniform pressure is applied and causes it to curve, and b) the sticky tape that is used to hold the samples on the wafer carrier causes non-uniformities in the sample-wafer carrier interface, resulting in irregular, random contact of the sample with the mask. Therefore, the successful photolithographic patterning of such small features using contact printing can only be achieved with a wafer process that guarantees a better contact of the substrate and the lithographic mask.

A new set of 4-inch chromium photolithographic masks for processing 3-inch wafers have been designed to include the test structures shown previously in figure 3.4, page 36. While darkfield polarity has been required, the delivered masks had a lightfield polarity. To correct the polarity, a AZ5214E image reversal resist and AZ726MIF bath developer from MicroChemicals GmbH has been used. For the UV exposure, the Karl Suss mask aligner has been used in the low vacuum contact mode (this mode applies 10^5Pa pressure between the wafer and the mask) that provides the best possible conformity of the wafer with the photolithographic mask. However, due to the high applied pressure and the presence of solvent in the photoresist, stiction occurred between the photoresist and the mask. To tackle this, the wafer with spun coated photoresist has been dipped in developer causing the conversion of the PGMEA solvent, at the surface of the photoresist thin film, into acetic acid which is not prone to stiction with the mask [42]. Using $1.4\mu\text{m}$ thick photoresist, the optimum photoresist exposure for $2\mu\text{m}$ line - $2\mu\text{m}$ space Wheatstone bridge features has been found to be 351mJoules . Diffraction patterns have been

observed to occur occasionally at the corners of the features, as shown in figure 3.7.

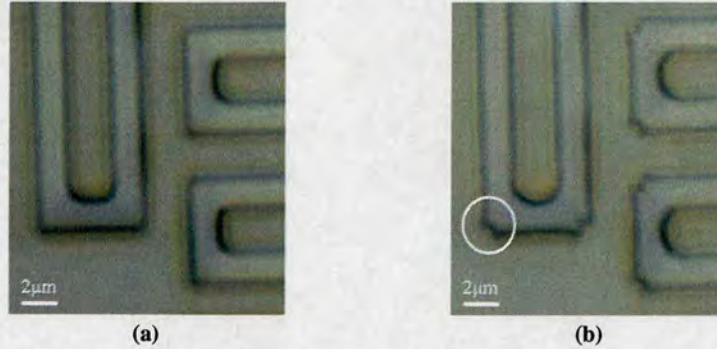


Figure 3.7: *Optical micrographs of printed features with a) no diffraction, and b) diffraction patterns present.*

Careful inspection of a few trial wafers has not revealed a correlation between the appearance of the diffraction patterns and particular positions on the wafers. Therefore, the appearance of these diffraction patterns in random locations should be due to non-uniformities in the photoresist thickness caused by particle contamination and/or the formation of micro-bubbles during the photoresist coating process. Following the characterisation of the photolithographic process, metallisation – p-type silicon circuits are fabricated next in section 3.4.

3.4 Fabrication of Wheatstone bridge, Kelvin resistor and metallic Greek cross circuits

Wheatstone bridge and Kelvin resistor microfeatures are fabricated by selective implantation of n-type crystalline silicon substrate with p-type boron, forming a p-n junction. Selective implantation of the substrate is achieved by deposition of an appropriate mask on the surface of the substrate, which is patterned to the desired shape of microfeatures prior to implantation. During implantation the patterned mask acts as selective ion stop layer where the ionic kinetic energy is transformed into thermal energy. The implication of this is that normal photoresist gets burned and SiO_2 that can be exposed to high temperature is required as implantation mask. Previously, in section 3.1, boron implantation at 30keV, 55keV and 80keV acceleration energies have been characterised. To determine the minimum SiO_2 layer thickness that is required to fully stop the boron ions for the acceleration energies used here, TRIM simulations have been performed for acceleration energies ranging between 10keV and 90keV. The maximum penetration of the ions

has been shown to be linearly related to the acceleration energy and, at 90keV, a 550nm thin SiO_2 film is required to fully stop the accelerated ions. Next the circuits are fabricated using the process illustrated in figure 3.8.

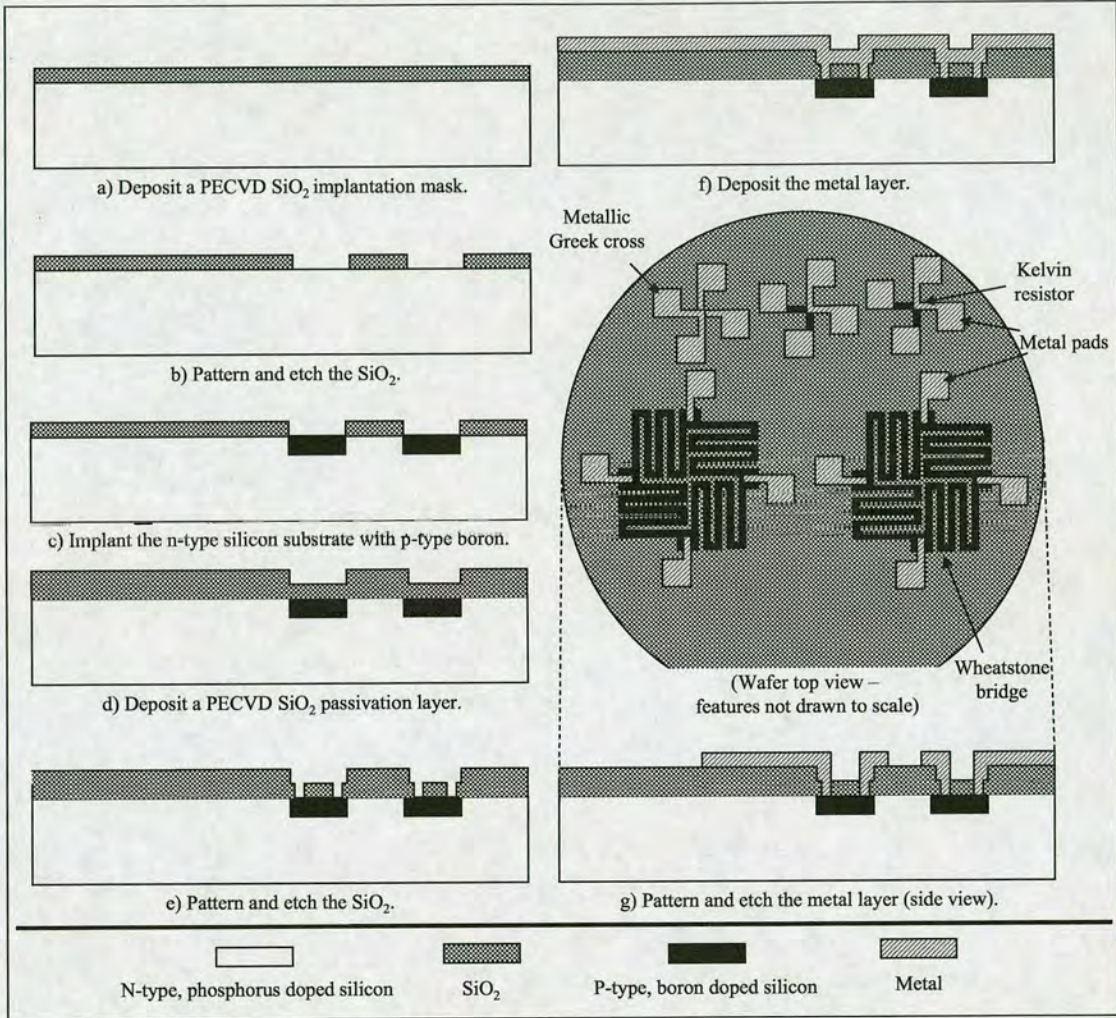


Figure 3.8: *Fabrication process of the electrical circuits.*

Initially a 550nm thin PECVD SiO_2 implantation mask has been deposited on the substrate (fig.3.8a). This SiO_2 mask is sufficient in stopping boron ions accelerated at energies up to 90keV. Next the wafers have been photolithographically patterned using 1:1 contact printing in a Karl Suss MA8/BA6 mask aligner, which is the tool used for process development in this thesis. For this process, a $1.3\mu\text{m}$ thin, i-line SPR350 photoresist from Shipley had been used. This photolithographic step prepared the samples for the subsequent etch step that would serve to remove the SiO_2 and create windows for the boron implantation. To etch the SiO_2 ,

CF₄/H₂ plasma has been employed in the Plasmatherm RIE parallel plate etcher (fig.3.8b). After the etch step, the photoresist has been removed in a fuming nitric acid solution and the substrates have been implanted with boron at 30keV, 55keV and 80keV acceleration energies, using 3.5×10^{13} atoms/cm² and 7×10^{15} atoms/cm² doses (fig.3.8c). This step has been followed by activation of the boron impurities at 1000°C for 35 minutes in N₂ environment. To prepare the wafers for the deposition of the metal film after the boron implantation and high temperature activation, additional 300nm thin PECVD SiO₂ passivation layer has been deposited on the substrate, on top of the 550nm thin PECVD SiO₂ implantation mask and on top of the implanted silicon regions (fig.3.8d). Next, the metal to silicon contact windows have been photolithographically patterned, the 300nm thin SiO₂ passivation layer has been dry etched in the Plasmatherm, in CF₄/H₂ plasma, revealing the underlying implanted silicon (fig.3.8e). After the completion of the etch process, the remaining photoresist has been stripped in O₂ plasma. Before the deposition of a metal layer, the wafers have been cleaned in a diluted 10:1:1 de-ionized water:hydrofluoric acid:hydrochloric acid solution for 5 to 10 seconds, have been rinsed with de-ionized water and have been blown dry with a N₂ gun. This step would serve to clean the native oxide on the silicon surface of the silicon – metal interfacial contacts. Immediately after the clean, the metallisation layer would be deposited on the substrate (fig.3.8f) and would contact the SiO₂ passivation layer. It would also contact selectively the p-type boron doped silicon at the predefined metal – semiconductor contact windows. When metal comes into contact with silicon solid state diffusion of silicon into the deposited metal may occur. This leaves voids in the silicon lattice, which may be subsequently filled by the metal during single or multiple sintering processes, causing effectively spikes of metal into the silicon. Because the spikes may short electrically shallow p-n junctions, the selected metallisation should minimize or hinder completely the silicon solid state diffusion process.

The metallisations fabricated here consist of a titanium nitride barrier layer -of unknown work function- followed by a titanium layer or an aluminium with 1 percent silicon layer. These metallisations minimize the silicon solid state diffusion and are compatible with our implanted boron doped microfeatures. After deposition on the substrate, the metallisations are patterned to define the electrodes and to complete the fabrication of Kelvin resistors, Wheatstone bridge circuits and Greek cross test structures. In the next two sections, two metallisations (titanium nitride/titanium and aluminium with one percent silicon) are fabricated and characterised electrically.

3.4.1 Titanium nitride and titanium metallisation

Titanium nitride has been found to be a stable diffusion barrier for silicon, for temperatures up to 500°C [43] or 600°C [44–46]. It acts as an excellent diffusion barrier and p-n junctions as shallow as 200nm for application in solar cells have been fabricated successfully [46]. The TiN diffusion barrier could be produced here by magnetron sputtering of a titanium target and the introduction of N₂ gas in the chamber of a Plasmalab 400 sputterer from Oxford Technology. Following the deposition of 25nm of titanium nitride, 500nm thin titanium film has been deposited on some samples (fig.3.8f). The deposition conditions can be found in table B.2, appendix B. After the completion of the deposition process, the wafers have been photolithographically patterned and etched to define the metal lines in a Surface Technology Systems metal etcher that employs SiCl₄/Ar plasma (fig.3.8g). The remaining photoresist has been completely removed in a O₂ plasma after a 60 minute process.

After completion of the fabrication process, the metallic Greek cross test structures have been electrically probed to investigate the electrical properties of the metallisation alone. Here the TiN thin film that has been exposed to O₂ plasma during the photoresist strip process has not been found to be conducting when electrically probed. This could be due to the fact that TiN reacted with the O₂ plasma to form a titanium oxynitride (TiO_xN_x) nonconducting layer. To test this hypothesis, the samples have been etched for additional 5 minutes in the metal etcher and have been found to be electrically conducting, implying that the TiO_xN_x layer had been removed. The resistivity of TiN has been measured to be $5.07m\Omega \cdot cm$. This value, being about 1 to 2 orders of magnitude larger than values found in the literature [45, 46], raises a suspicion on the stoichiometry of TiN film deposited here.

To test the electrical characteristics of the interfacial contacts between TiN diffusion barrier and p-type boron doped silicon, the Kelvin test resistors with metal – p-type semiconductor interfacial contact areas of $3\mu m^2$, $5\mu m^2$ and $10\mu m^2$ have been electrically probed. The contacts have been found to have non-linear current-voltage characteristics, shown in the graph in figure 3.9.

Research on TiN and silicon Schottky barrier height has shown that for d.c. magnetron sputtered TiN, an anneal process with temperature up to 600°C, in vacuum, with duration of 15 minutes could reduce the barrier height. Here the samples that included a TiN and Ti metal layer have been annealed at 425°C, 500°C and 600°C in N₂ environment for 35 minutes. The interfacial contact current-voltage characteristics have not been altered after sample annealing

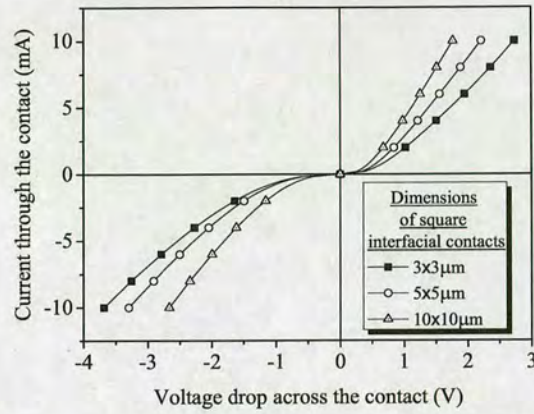


Figure 3.9: *Interfacial metal – semiconductor contact current-voltage curves of TiN deposited on boron doped p-type crystalline silicon, obtained by probing Kelvin resistors. The boron implantation energy has been 55keV and the dose has been 7×10^{15} atoms/cm², activated at 1000°C for 35 minutes.*

at 425°C. The metal film of the samples that have been annealed at 500°C has been found to be nonconducting, while the metal film of the samples that have been treated at 600°C readily peeled off from the substrate when probed. Due to failure to produce TiN-Ti metal–p-type silicon ohmic contacts, aluminium metallisation is attempted next.

3.4.2 Aluminium with 1 percent silicon metallisation

Plain aluminium films suffer from limitations when used as metallisation for direct contact with silicon. During sinter steps that aim to rectify metal – semiconductor contacts, silicon dissolves in the aluminium leaving voids that are filled by the metal, causing metal spikes into the substrate. These can short p-n junctions as deep as 1μm [47], rendering pure aluminium incompatible with our implants because the p-n junctions here occur at approximately 0.6μm depth (see figure 3.2a). The silicon to metal solid diffusion and its side effects can be minimized by adding a small amount of silicon into aluminium. Aluminium with about 1 percent silicon has been one of the most popular metals for VLSI circuits and has been extensively studied [48].

This metal – silicon alloy, which limits diffusion of silicon, has also been available here for deposition by magnetron sputtering. This alloy has been reported in the literature to be used to fabricate devices with junction depth of 0.3μm [49]. From the boron distribution curves seen

in figure 3.2a, page 33, it is observed that the p-n junctions for the implantation conditions here occur at $0.6\mu\text{m}$ approximate depth, hence the fabrication of Al-1%Si-p-type silicon contacts should be successful here.

500nm thin Al-1%Si metal alloy has been deposited here in a Balzers magnetron sputter system (fig.3.8f), it has been patterned and etched in the Surface Technology Systems metal etcher (fig.3.8g) using SiCl_4/Ar plasma. The photoresist has not been removed straight away, but instead the samples have been left in the atmosphere overnight and the photoresist was removed in an O_2 plasma the next day. Inspection with a scanning electron microscope revealed that the metal layer have been corroded. Figure 3.10 shows selected electron microscope images. The

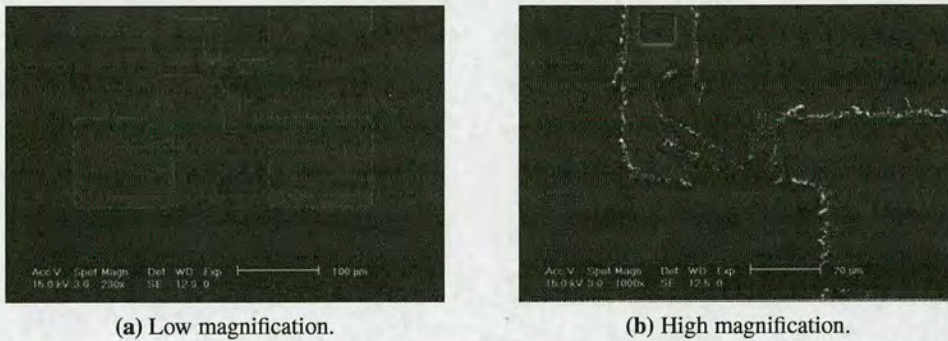


Figure 3.10: Scanning electron microscope images of corroded aluminium - 1% silicon alloy.

corrosion is believed to be the result of the reaction of the metal with hydrochloric acid (HCl), according to the reaction: $2\text{Al(s)} + 6\text{HCl(aq)} \Rightarrow 2\text{AlCl}_3\text{(s)} + 3\text{H}_2\text{(g)}$. The HCl acid must have been formed by the combination of Cl_2 , which is a residual byproduct of the metal etch step and was trapped in the photoresist, with atmospheric H_2O . New wafer samples have been prepared and stripping the photoresist in an O_2 plasma directly after the metal etch step has been found to solve the corrosion problem.

After patterning the metallisation, a sinter step is necessary to form ohmic metal – semiconductor contacts. For the aluminium-1% silicon alloy sintering temperatures up to 450°C have been shown to reduce the metal – semiconductor contact resistance [49]. Here, sinter processes at 300°C (15, 30 and 60 minutes duration) and 435°C (15 and 30 minutes duration) temperatures in H_2/N_2 forming gas have been performed.

To test the electrical characteristics of the interface between aluminium-1% silicon metallisation and p-type boron doped silicon, the Kelvin test resistors with metal – semiconductors

interfacial contact areas of $10\mu\text{m}^2$ have been electrically probed before and after each sinter step. The current voltage characteristics of the metal – semiconductor interfacial contacts before and after each sinter step for 300°C sinter temperature are shown in figure 3.11a. As can be seen in figure 3.11a, sintering at 300°C has not produced linear ohmic metal – semiconductor contacts even after 60 minute long sinter step. However, it can be seen in figure 3.11b that sintering at 435°C for 30 minutes has produced linear current-voltage electrical curves implying that ohmic metal – semiconductor contacts have been achieved. From figure 3.11b, the specific contact resistivity of ohmic Al-1%Si–boron doped semiconductor contacts after sintering at 435°C for 30 minutes has been calculated to be $1.32\mu\Omega/\mu\text{m}^2$.

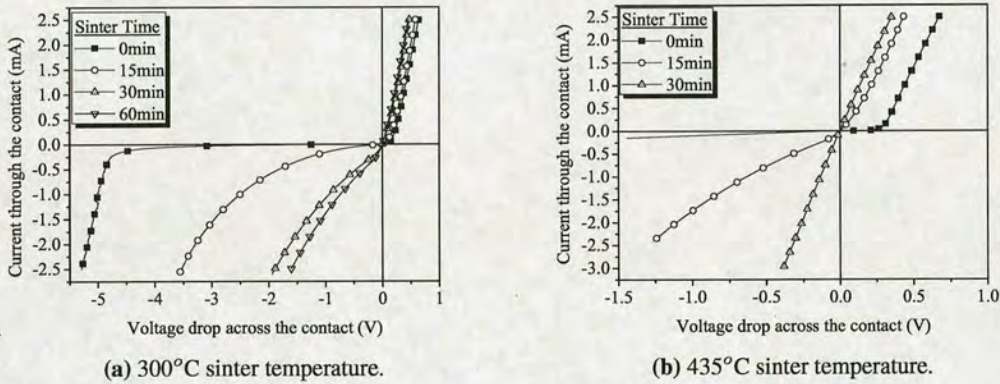


Figure 3.11: Current-voltage curve of Al-1%Si and boron doped p-type crystalline silicon interfacial contacts, obtained by probing Kelvin resistors. The boron implantation energy has been 30keV and the dose has been $3.5 \times 10^{13}\text{atoms}/\text{cm}^2$, activated at 1000°C for 35 minutes. The interfacial contact area is $10\mu\text{m}^2$.

The resistivity of aluminium-1% silicon metallisation layer has been measured using Greek cross test structures. Prior to sintering, the resistivity of the metal layer has been measured to be $5.5\mu\Omega\cdot\text{cm}$ and reduced to $3.2\mu\Omega\cdot\text{cm}$ after 30 minute long sinter step at 435°C .

3.4.3 Characterisation of the Wheatstone bridge electrical characteristics

After completion of the fabrication process that includes selective p-type boron implantation ($55\text{keV} - 7 \times 10^{15}\text{atoms}/\text{cm}^2$ and $30\text{keV} - 3.5 \times 10^{13}\text{atoms}/\text{cm}^2$) in n-type silicon substrate, deposition of SiO_2 passivation on top of the implanted microfeatures, patterning of metal – semiconductor contact windows in the SiO_2 passivation layer, deposition and pattern of metallisations (TiN/Ti and Al-1%Si) and characterisation of metal – semiconductor contacts by

probing electrically Kelvin resistors, the electrical properties of Wheatstone bridge circuits (resistance and offset voltage) are characterised.

The fabrication parameters are listed in table 3.1. The Wheatstone bridge test circuits have been probed electrically to determine the effect of the process variations in the bridge resistances and offset voltages. The results obtained from electrical tests are plotted in figure 3.12, where the vertical error bars indicate the standard deviation across the electrical measurements.

Sub-process	A	B
Implantation Energy	30keV	55keV
Implantation Dose	3.5×10^{13}	7×10^{15}
Metallisation	Al-1%Si	TiN/Ti
Sinter	435°C, 30 minutes, H ₂ /N ₂ gas	No
Linear current voltage characteristics	Yes	No
Wheatstone bridge resistance and offset voltage uniformity	Worse	Better

Table 3.1: Fabrication process and electrical characteristics of sub-process A and B.

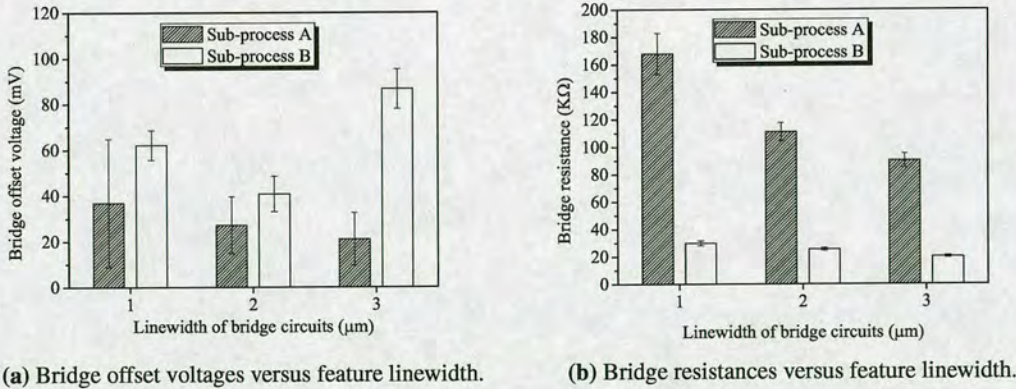


Figure 3.12: Electrical characteristics of the fabricated Wheatstone bridges at +3.3V bias, as a function of feature linewidth. The vertical error bars indicate the standard deviation across the sample measurements. The bridge layouts are shown in figure 3.4.

The variation in the Wheatstone bridge offset voltages with respect to linewidth of serpentine shaped Wheatstone bridge features for fabrication sub-processes A and B can be seen in figure 3.12a. The offset voltages of bridge circuits fabricated with sub-process A show higher standard deviation compared to sub-process B. For sub-process A, the standard deviation decreases as the microfeature linewidth increases, whereas this trend is not observed for sub-process B.

The variation in the Wheatstone bridge resistances with respect to the linewidth of the Wheatstone bridge serpentine shaped microfeatures can be seen in figure 3.12b. Circuits fabricated with sub-process A demonstrate declining standard deviation as the resistor linewidth increases. Furthermore, devices fabricated with sub-process A yields higher Wheatstone bridge spread in the resistance, as indicated by the standard deviation error bars.

3.5 Conclusion

In section 3.1 the distribution profiles and sheet resistances of implanted and activated boron have been characterised by secondary ion mass spectroscopy, TSUPREM4 simulations and experimentally obtained 4-point probe measurements. For implantation in blank silicon, the simulated distribution profiles and sheet resistances have been in good agreement with experimental SIMS results and sheet resistance measurements. A small deviation between simulated and experimentally obtained sheet resistances indicates that boron may not have been fully activated; this however should not have a negative impact in the piezoresistive properties of boron implanted silicon.

In section 3.2 the test structures that include metallic Greek crosses for electrical characterisation of the metallisation, Kelvin resistors for the characterisation of metal – semiconductor interfacial contacts and serpentine shaped Wheatstone bridge circuits for characterisation of their resistance and offset voltage have been presented.

In section 3.3 the lithographic process has been characterised. It has been found that small features with $2\mu\text{m}$ line-space geometry cannot be printed on silicon shards, but transferring the lithographic process on wafer scale has been successful in printing small size features.

Greek crosses, Kelvin resistors and serpentine shaped Wheatstone bridges have been fabricated by implantation of p-type boron in n-type silicon and have been integrated with TiN-Ti and Al-1%Si electrodes. TiN-Ti-boron doped crystalline silicon interfacial contacts have not been found to be ohmic, as opposed to Al-1%Si metal alloy-boron doped crystalline silicon that yielded ohmic interfacial contacts after sintering at 435°C for 30 minutes in N_2/H_2 environment, and has been chosen as the metallisation for the MEM devices.

Chapter 4

First design iteration: integration of full-active Wheatstone bridge circuits with silicon cantilever beams

The MEM air flow sensor fabricated in this project consists of: a) Wheatstone bridge circuits made of a patterned metallisation and p-type boron doped microfeatures implanted in n-type single crystalline silicon, b) silicon cantilever beams that are integrated with the full-active Wheatstone bridge circuits, and c) out of plane flaps that are integrated at the free end of silicon cantilever beams.

In chapter 3 Wheatstone bridge circuits have been fabricated by implantation of p-type boron doped microfeatures in single crystalline n-type silicon. The p-type Wheatstone bridge microfeatures have been integrated with metallic Al-1%Si electrodes and have been electrically characterised.

In this chapter is presented the second phase of the development process of the MEM system, which aims to integrate the Wheatstone bridge circuits with micromachined silicon cantilever beams. 4-inch silicon on insulator (SOI) wafers have been used for this purpose. In section 4.1 the SOI wafer specifications, the fabrication process summary and the design layout of the devices is presented. In section 4.2 the fabrication of the Wheatstone bridge circuits consisting of piezoresistive p-type microfeatures (in the device layer of SOI wafers) and patterned metallisation is presented.

The integration of electrical circuits with micromachined silicon cantilever beams, which are released with wet (section 4.3) and dry (section 4.4) bulk micromachining methods, is developed. Once the fabrication process has been complete and the Wheatstone bridge circuits have been integrated with micromachined silicon cantilever beams, the devices have been probed electrically to investigate their performance in section 4.5.

4.1 Wafer specification and design layout

As mentioned previously, the silicon on insulator wafer with specifications listed in table 4.1 has been chosen for the fabrication of the MEM devices. The silicon on insulator wafer has been

Type	Dopant	Concentration (atoms/cm ³)	Sheet Resistance	Thickness μm	Function
Silicon device layer	Phosphorus	7.43×10^{14}	$4\text{K}\Omega/\square$	15	Electrical circuits Cantilever beams
Buried SiO ₂	-	-	-	2	Etch stop
Silicon handle wafer	Phosphorus	Not measured	Not measured	425	Support
Thermal SiO ₂ (polished)	-	-	-	2	Etch mask

Table 4.1: Silicon on insulator wafer specification. The substrate diameter is 4 inches.

chosen because the silicon in the device layer and the handle wafer can be etched independently using the buried oxide as an etch stop layer.

Initially the circuits (p-type Wheatstone bridge integrated with metallic electrodes) are fabricated in the device layer of the SOI wafer. Summary of the fabrication process for the electrical circuits can be seen in figure 4.2, page 52.

Following the fabrication of the electrical circuits, the wafers are micromachined to define and release the cantilevers. The cantilevers are defined in the device layer of the SOI wafer by a dry etch micromachining step where the buried oxide is used as an etch stop. To release the cantilevers, windows are defined on the backside of the wafer and the polished thermal SiO₂ on the backside of the substrate is dry etched to reveal the silicon handle wafer and prepare the substrate for deep micromachining, which can be performed by wet or dry etching. Summaries of the micromachining processes, including the definition of cantilever beams with dry etch and their subsequent release with wet or dry bulk micromachining, can be seen in figure 4.3, page 53 and figure 4.5, page 56 respectively. As can be seen in each figure, deep micromachining serves to remove the bulk silicon beneath the defined cantilevers to allow the release of cantilever beams.

The field layout of the MEM devices fabricated in this chapter can be seen in figure 4.1. The design includes fourteen silicon cantilever beams defined by a dry etch step in the device layer of SOI wafer. The length of the cantilever beams ranges from $200\mu\text{m}$ to $1000\mu\text{m}$ and the widths have been $200\mu\text{m}$ and $300\mu\text{m}$. Most cantilever beams include stress concentration regions

First design iteration: integration of full-active Wheatstone bridge circuits with silicon cantilever beams

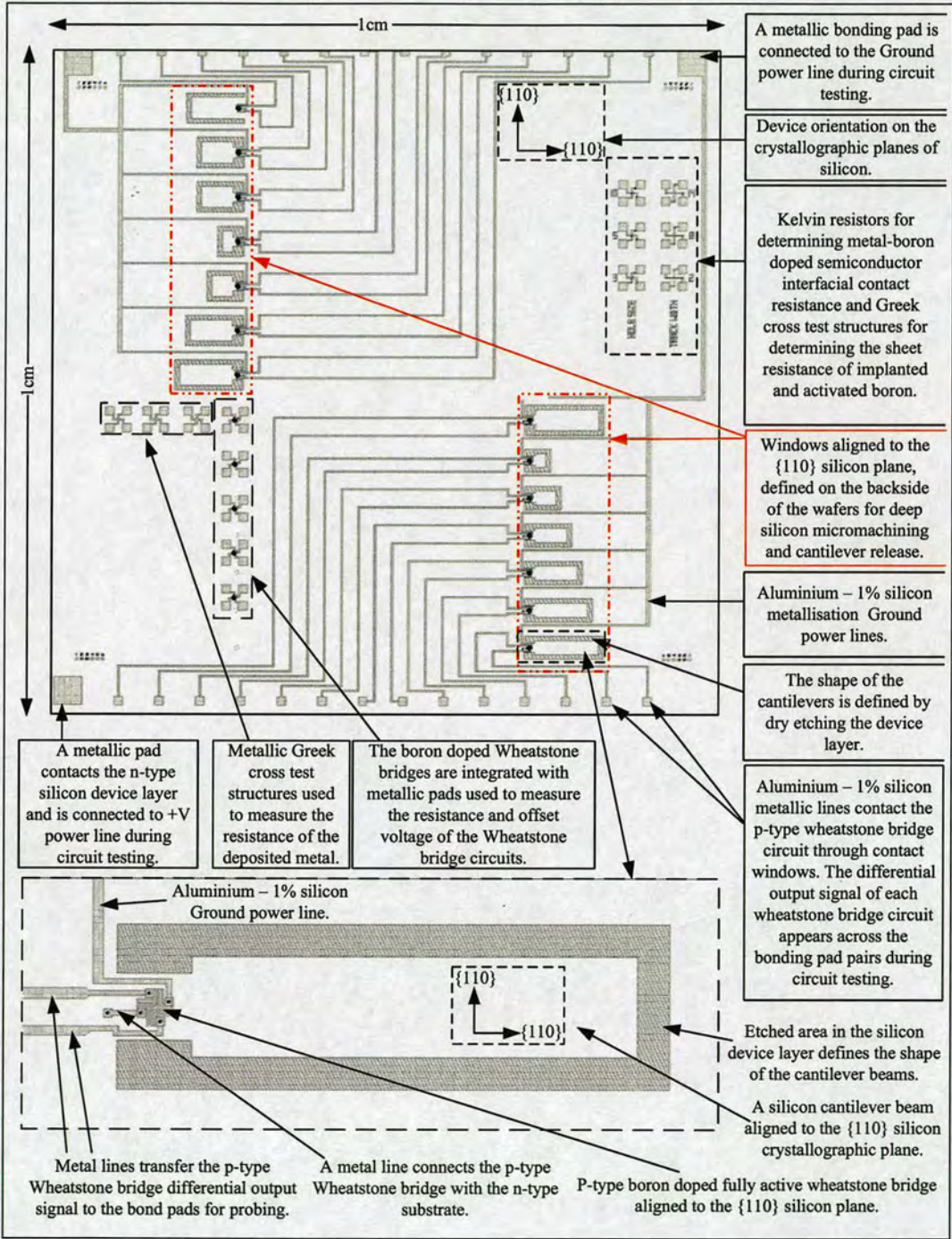


Figure 4.1: Field layout of the MEM devices fabricated in the first design iteration.

135 μm wide and 150 μm long, where full-active Wheatstone bridge circuits are defined by boron implantation. A single metallisation layer of patterned aluminium with 1 percent silicon has been used for integration with the Wheatstone bridge circuits. For the release of silicon cantilever beams, the SiO_2 layer on the backside of the wafer has been selectively removed to define large windows. Using the SiO_2 as etch mask, the silicon handle wafer is bulk etched using wet or dry micromachining. After the completion of the fabrication process, the cantilever beams integrated with Wheatstone bridge circuits can move freely when perturbed, causing a change ΔR in the four piezoresistive arms of the Wheatstone bridge, hence a differential output voltage ΔV , which is detected by probing the metallic bonding pads.

The fabrication process (electrical circuits and integration with micromachined cantilever beams) is described in this chapter, starting with the fabrication of the electrical circuits next in section 4.2.

4.2 Fabrication of the electrical components

The fabrication of p-type boron strain gauges by implantation of boron in n-type single crystalline silicon and their integration with metallisation is shown in figure 4.2. This process has been characterised previously in chapter 3.

First a 0.55 μm thin SiO_2 layer that acts as implantation mask is deposited on the silicon on insulator substrate (fig.4.2a). Next, the substrate is patterned photolithographically and the SiO_2 implantation mask is dry etched in a CF_4/H_2 plasma to define the windows for boron implantation (fig.4.2b). After the removal of the photoresist in O_2 plasma, the wafers have been implanted with boron at Ion Beam Services. The implantation energy has been 55keV and the dose has been $3.5 \times 10^{13} \text{atoms/cm}^2$ (fig.4.2c). Next, the implanted boron has been activated at 1000°C for 35 minutes in N_2 atmosphere. After activation, a 0.3 μm thick SiO_2 passivation layer has been deposited on top of the existing SiO_2 implantation mask and on top of the boron implanted areas (fig.4.2d) to insulate the implanted regions from the metallisation which is deposited later in the process. The contact windows have been patterned photolithographically and the SiO_2 has been etched in CF_4/H_2 plasma (fig.4.2e). Finally a 0.5 μm thick aluminium 1 percent silicon alloy is deposited on the substrate using magnetron sputtering, it is patterned lithographically and the metallic lines and contact pads are defined using wet etchant from Rockwood (fig.4.2f).



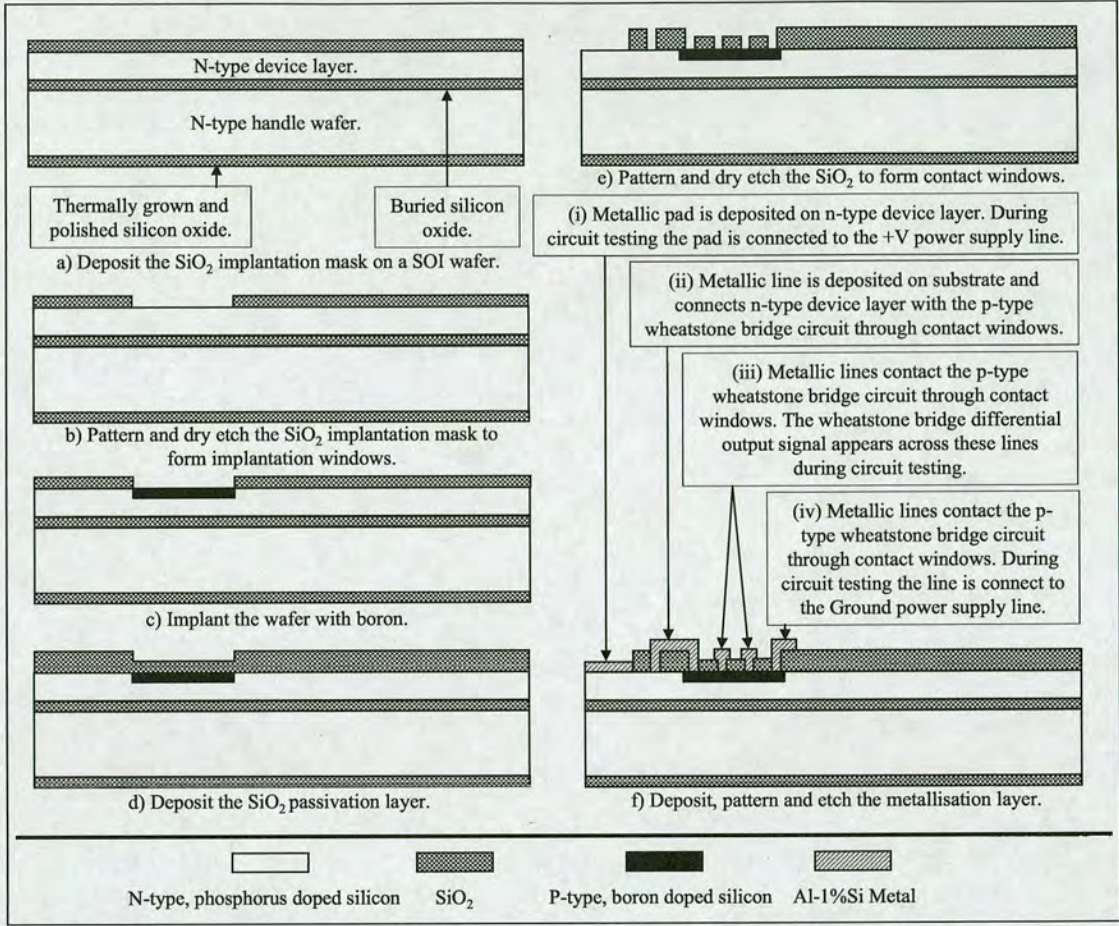


Figure 4.2: Fabrication of p-type boron strain gauges and metallisation on silicon on insulator wafer.

As can be seen in figure 4.2f(i), one metallic pad per die is deposited directly on the silicon substrate and during the electrical characterisation of the devices this pad is connected to the +V line of the power supply. Additional metallic lines that carry the differential output signal of the Wheatstone bridge can be seen in figure 4.2f(ii,iii). An additional metallic line seen in figure 4.2f(iv) is connected through a contact window to the Wheatstone bridge and during the electrical characterisation of the devices this line is connected to the Ground line of the power supply.

After the fabrication of the electrical components, the cantilevers have to be fabricated and integrated with the strain gauges. The fabrication of the cantilevers using wet and dry micro-machining processes is described next in sections 4.3 and 4.4 respectively.

4.3 Bulk micromachining by wet etching

Tetramethyl ammonium hydroxide (TMAH) and potassium hydroxide (KOH) are widely used to etch silicon anisotropically [50, 51]. Here, a TMAH solution has been used for bulk micromachining of the wafers because the existing thermal oxide on the handle wafer could act as etch mask. The etch selectivity of the thermal SiO_2 to silicon at 4wt.% TMAH solution at 80°C has been reported to be 5.3×10^3 [50]. The smoothness of the etched sidewalls and the accurate control of the $\{100\}/\{111\}$ plane etch selectivity have not been critical for the process here, and a surfactant that could modify the aforementioned etch characteristics was not required [51].

The micromachining process here continues from the point where the electrical components (p-type strain gauges and metallisation) have been fabricated, as shown in section 4.2, figure 4.2f.

The micromachining process that includes a wet bulk etch step is illustrated in figure 4.3.

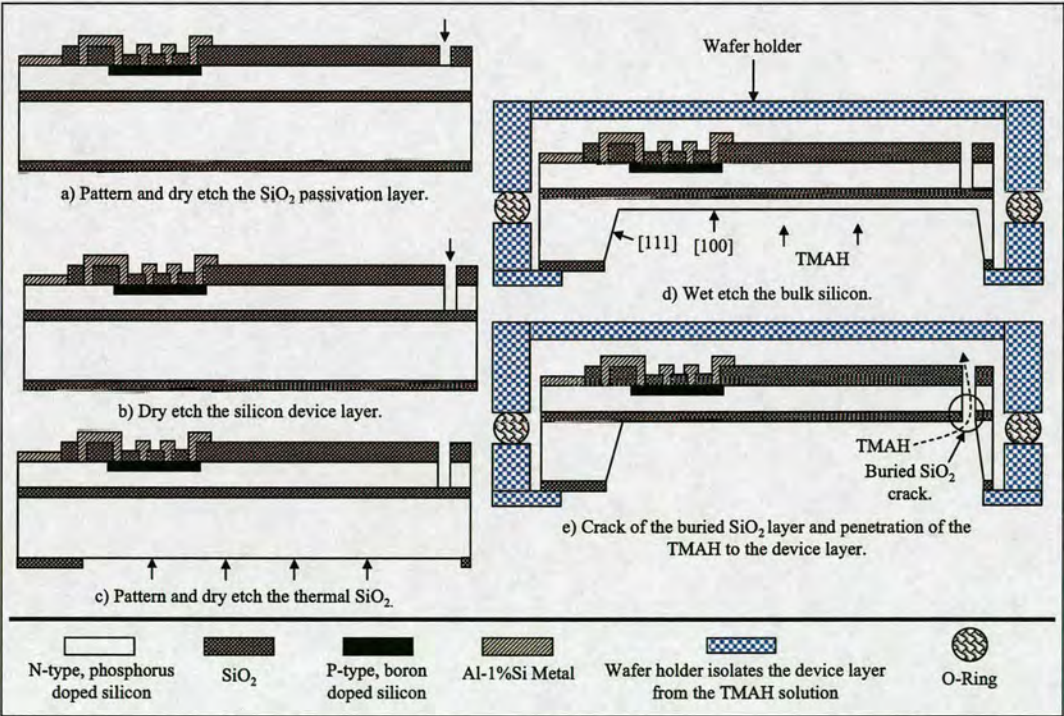


Figure 4.3: Process for the fabrication of the microcantilever beams using wet bulk micromachining. The arrows indicate the location of the etch.

Initially the device layer of the wafers has been photolithographically patterned to define the

cantilevers and the SiO_2 passivation layer has been etched in the Plasmatherm (fig. 4.3a). The silicon device layer has been subsequently etched highly anisotropically in the ICP reactor using Bosch process 'A' (fig. 4.3b) (Bosch process details can be found in appendix B, table B.3).

Subsequently the handle wafer has been processed. The thermal SiO_2 on the backside of the wafer is dry etched in CF_4/H_2 plasma (fig. 4.3c) to prepare the wafer for wet bulk micromachining step. For this step a Protek B coating layer from Brewer Science that offers protection from alkaline or acidic solutions, including TMAH, has been spun coated and thermally cured on the device layer with a soft bake step on hot plate.

A 3 liter solution consisting of 21% volume TMAH and de-ionized H_2O has been heated to 90°C . A holder that has been designed to isolate the device layer of the wafers during the wet etch has been used here. The wafers that have been mounted to the wafer holder, have been placed in the heated TMAH solution and the wet etch commenced (fig. 4.3d). The TMAH solution has been agitated during the etch process and the concentration of the solution has been maintained constant by adding de-ionized water to replenish the quantity that has been evaporated. The etch lasted for approximately 7 hours, yielding a $\{100\}$ plane etch rate of approximately $1\mu\text{m}/\text{min}$. Figure 4.4a shows a low magnification view of the cross section of an etched cavity. The scanning electron microscope image shown in figure 4.4b illustrates the etch of the $\{111\}$ plane by $12\mu\text{m}$, yielding a $\{100\}/\{111\}$ plane etch selectivity of 35.

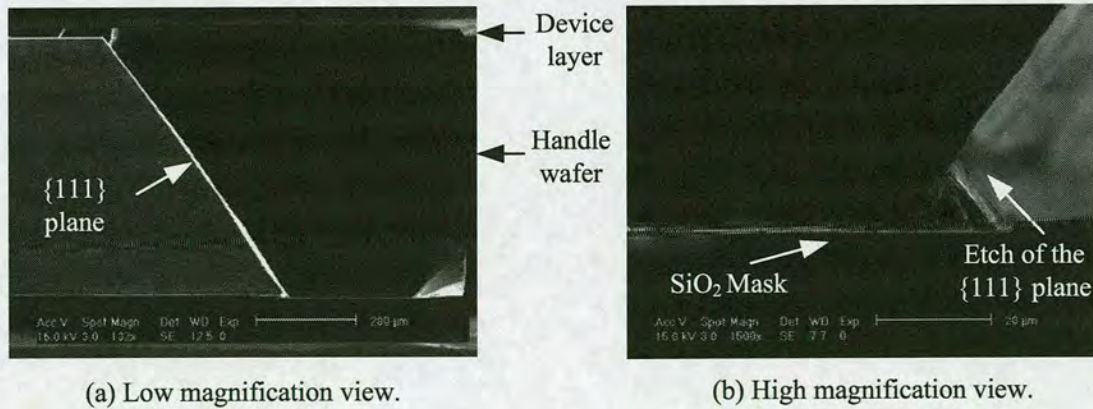


Figure 4.4: Scanning electron microscope images of the cross section of the wet etched handle wafer.

Because these SOI wafers have been fabricated by a high temperature bonding process, the

difference in the thermal expansion coefficients α_i of silicon ($2.3 \times 10^{-6}/\text{K}$ [52]) and SiO_2 ($0.5 \times 10^{-6}/\text{K}$ [53]) result in thermal stresses that develop as the wafers cool down to room temperature after the bonding process [54]. The stress between the silicon of the device layer and the buried silicon oxide have caused the SiO_2 to crack (indicated by the arrow and the circle in figure 4.3e), thus allowing the wet etchant to access the device layer.

The Protek B protective coating has not proved to be effective as it lifted off, allowing etching of the metal layer and partly of the device layer that constitutes the microstructures. Since the wet micromachining process has been unsuccessful, a dry etch approach has been attempted next in section 4.4.

4.4 Bulk micromachining by dry etching

For dry micromachining of silicon substrates deep reactive ion etching (DRIE) is commonly employed in ICP reactor systems using Bosch processes that can achieve highly anisotropic etch profiles. A key characteristic of a Bosch etch process is the cyclic etch and passivation steps. During the etch cycle a SF_6/O_2 plasma etches pre-patterned silicon substrate, forming trench in the substrate. During the passivation cycle a C_4F_8 plasma passivates the substrate with a C_xF_y polymer. In the next etch cycle the passivation at the bottom of a trench is quickly removed due to ion bombardment, revealing the underlying silicon that is etched quickly due to exposure to ion bombardment and fluorine radicals. The ions attack the trench sidewalls at a much slower rate which is not sufficient to remove the polymer passivation. As result the passivation protects the silicon sidewalls from exposure to fluorine radicals and etch anisotropy is achieved.

The dry micromachining process continues from the point where the electrical components (p-type strain gauges and metallisation) have been fabricated in section 4.2, figure 4.2f. The plasma based micromachining process developed here is illustrated in figure 4.5.

Initially the wafers have been patterned photolithographically to define the cantilevers. For this step a $7\mu\text{m}$ thick photoresist SPR220.7 from Shipley has been used. Next, the SiO_2 passivation layer has been completely etched in a Plasmatherm (fig. 4.5a), followed by a dry etch of the device layer (fig. 4.5b) using the bosch process 'A' (Bosch process work conditions are listed in table B.3, appendix B), revealing the underlying $2\mu\text{m}$ thick buried oxide layer. The buried SiO_2 has been consequently etched in the Plasmatherm, revealing the handle wafer (fig. 4.5c). Next,

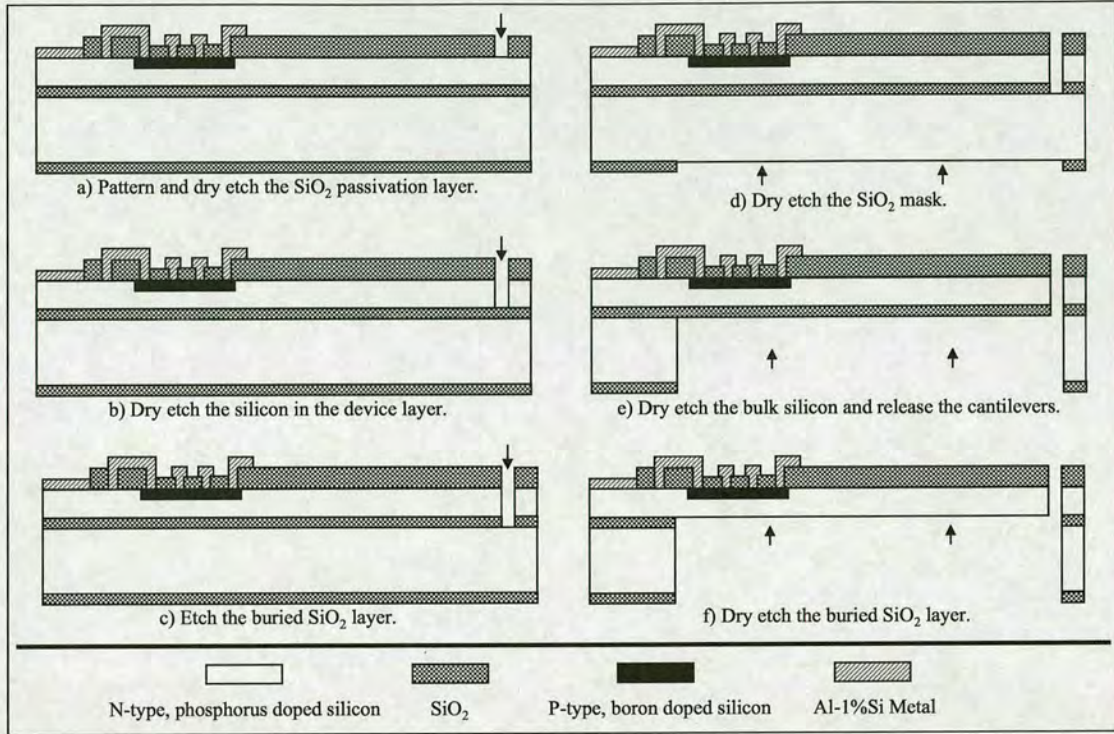


Figure 4.5: Process for the fabrication of the microcantilevers using a dry etch micromachining process. The arrows indicate the location of the etch.

the back side of the wafer has been photolithographically patterned with SPR220.7 photoresist. The SiO_2 masking layer has been etched in the Plasmatherm (fig. 4.5d) to prepare the substrate for the DRIE process. Subsequently the handle wafer has been etched in the ICP reactor (fig. 4.5e) using Bosch process 'A'.

Once the handle wafer has been etched and the structures have been released, the thermal stress in the Si- SiO_2 composite beam -discussed in section 4.3- was relaxed, causing a lateral deflection of the beams toward the bulk substrate. The removal of the buried silicon oxide thin film using a CF_4/H_2 dry etch step in the Plasmatherm (fig.4.5f) eliminated the source of strain and allowed the cantilevers to return to horizontal position. Although the high frequency PECVD SiO_2 which forms the passivation layer on top of the cantilevers has been compressively stressed, it did not cause a considerable deflection of the microstructures. A SEM image of the top view of a $750\mu\text{m}$ -long- $300\mu\text{m}$ -wide cantilever beam integrated with p-type boron doped piezoresistive Wheatstone bridge and patterned metallisation is shown in figure 4.6. The length and width of the cantilever at the stress concentration region is $150\mu\text{m}$ and $130\mu\text{m}$ respectively. The Wheatstone bridge strain gauges have $2\mu\text{m}$ line-space geometry.

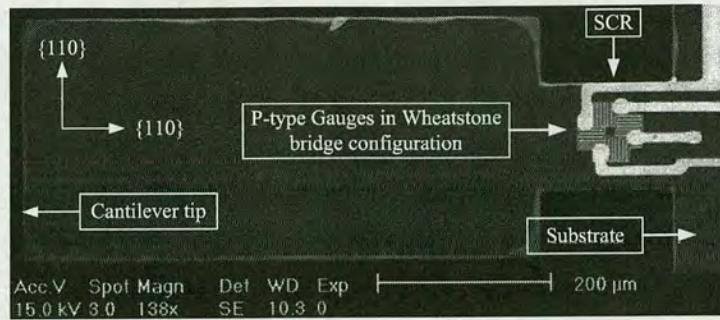


Figure 4.6: A scanning electron micrograph of the top view of a 750µm-long-300µm-wide cantilever beam integrated with p-type boron doped piezoresistive Wheatstone bridge and patterned metallisation. The length and width of the cantilever at the stress concentration region is 150µm and 130µm respectively. The piezoresistors have 2µm line-space geometry.

4.5 Electrical characterisation of the fabricated devices

Following the successful fabrication of the cantilever beams using the dry deep reactive ion etch micromachining process and their integration with the piezoresistive p-type Wheatstone bridge circuits, the devices have been tested electrically by probing the metallic pads. In section 4.5.1 the n-type device layer has been probed and it has been found that Schottky barriers are established at n-type semiconductor – metal contacts. In section 4.5.2 the n-type device layer and the p-type Wheatstone bridge have been electrically probed and the circuit has shown non-linear electrical characteristics. The p-type Wheatstone bridge circuits integrated with the cantilever beams have been probed directly in section 4.5.3 and the circuit has been found to produce a differential signal output when a cantilever beam has been deformed mechanically.

4.5.1 Probing the n-type device layer

As mentioned in section 4.2, each device carries one metallic pad which is connected to the +V power line during circuit testing. This has been shown previously in figure 4.2f. Before dicing the wafers in individual die, these metallic pads on adjacent devices have been probed electrically to obtain metal – n-type silicon (SOI device layer) current-voltage characteristics. The distance between the pads has been 1cm and the cross section of the effective electrical circuit being tested is shown in figure 4.7a. As can be seen, ohmic contacts between the metallic Al-1%Si pads and the n-type device layer could not be established due to the low intrinsic phosphorus concentration (7.43×10^{14} atoms per cm^3) of the device layer. The resulting metal – n-type semiconductor contacts have Schottky type current-voltage characteristics.

The diodes are connected in series with the n-type device layer which acts effectively as a resistor with $4\text{K}\Omega/\square$ sheet resistance. The circuit shown in figure 4.7a has been probed electrically and the obtained non-linear current-voltage electrical characteristics have been plotted in figure 4.7b. Next the p-type Wheatstone bridge that has been integrated with cantilever beams is supplied with current through the n-type device layer.

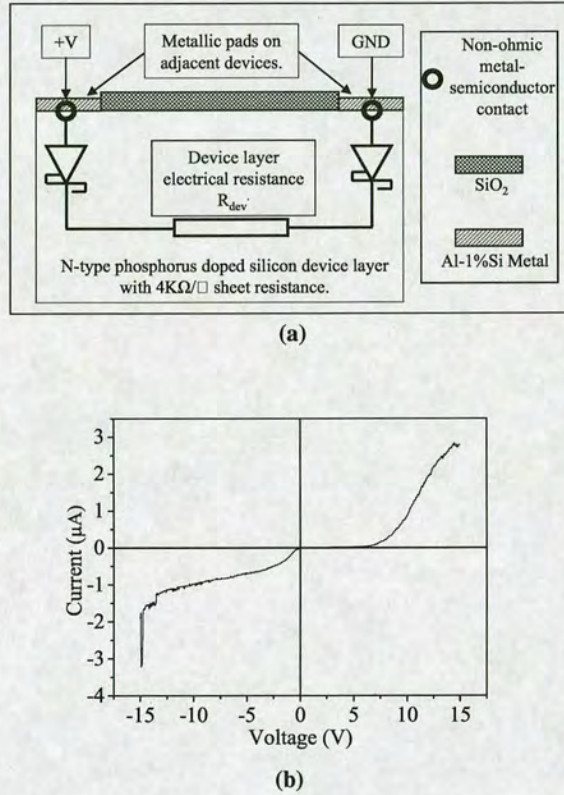


Figure 4.7: a) Aluminium – n-type semiconductor – aluminium electrical circuit and b) its current-voltage characteristic curve.

4.5.2 Probing the n-type device layer and the p-type boron implanted Wheatstone bridge

The cross section of a fabricated device including the cantilever beam, the p-type boron doped piezoresistive Wheatstone bridge and the patterned metallisation layer is shown in figure 4.8. The electrical setup including the current flow through the device during circuit testing is shown in the top part of figure. The detailed electrical circuit and the probing setup during testing is shown in the lower part of figure 4.8.

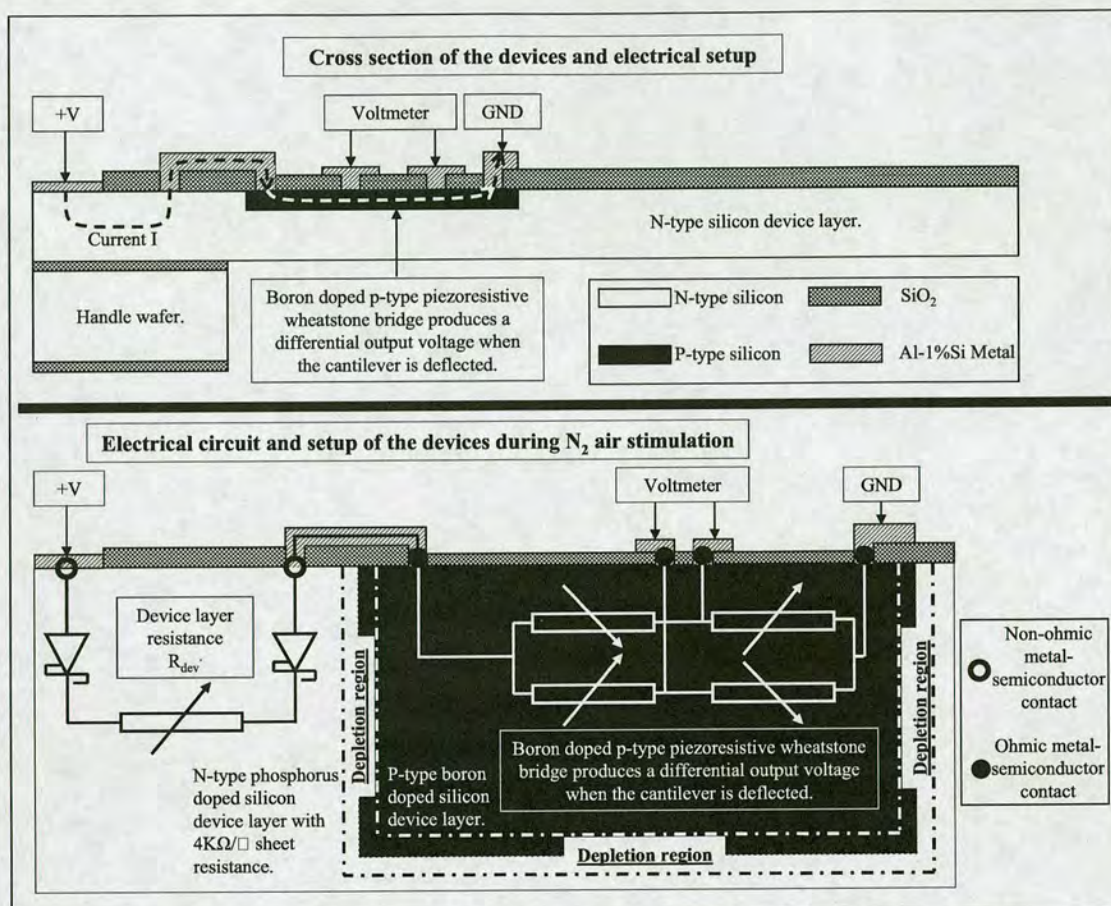


Figure 4.8: Top part: cross section of the devices, electrical setup and current flow during device testing. Lower part: electrical circuit of the devices.

During the electrical operation of the circuit, the metallic pad that has been deposited on the n-type silicon device layer is connected to the +V line of the power supply. The current flows through the metal – n-type semiconductor Schottky diode and into the n-type device layer with $4K\Omega/\square$ sheet resistance. Next, it flows through an additional n-type semiconductor – metal Schottky diode and into the metallic interconnect. The current flow continues through the p-type boron doped Wheatstone bridge circuit. As mentioned in section 4.2, the boron implantation energy has been 55keV, the dose has been 3.5×10^{13} atoms/cm², the samples have been sintered at 435°C for 30 minutes, forming ohmic metal – p-type semiconductor contacts, which is desirable. However, a potential barrier exists between the n-type and p-type doped semiconductors of the circuit due to their difference in the fermi levels, causing the circuit effectively to act as a p-n junction operated in reverse bias. Next the current flows through the Wheatstone bridge and terminates in the Ground terminal. The devices have been tested electrically and

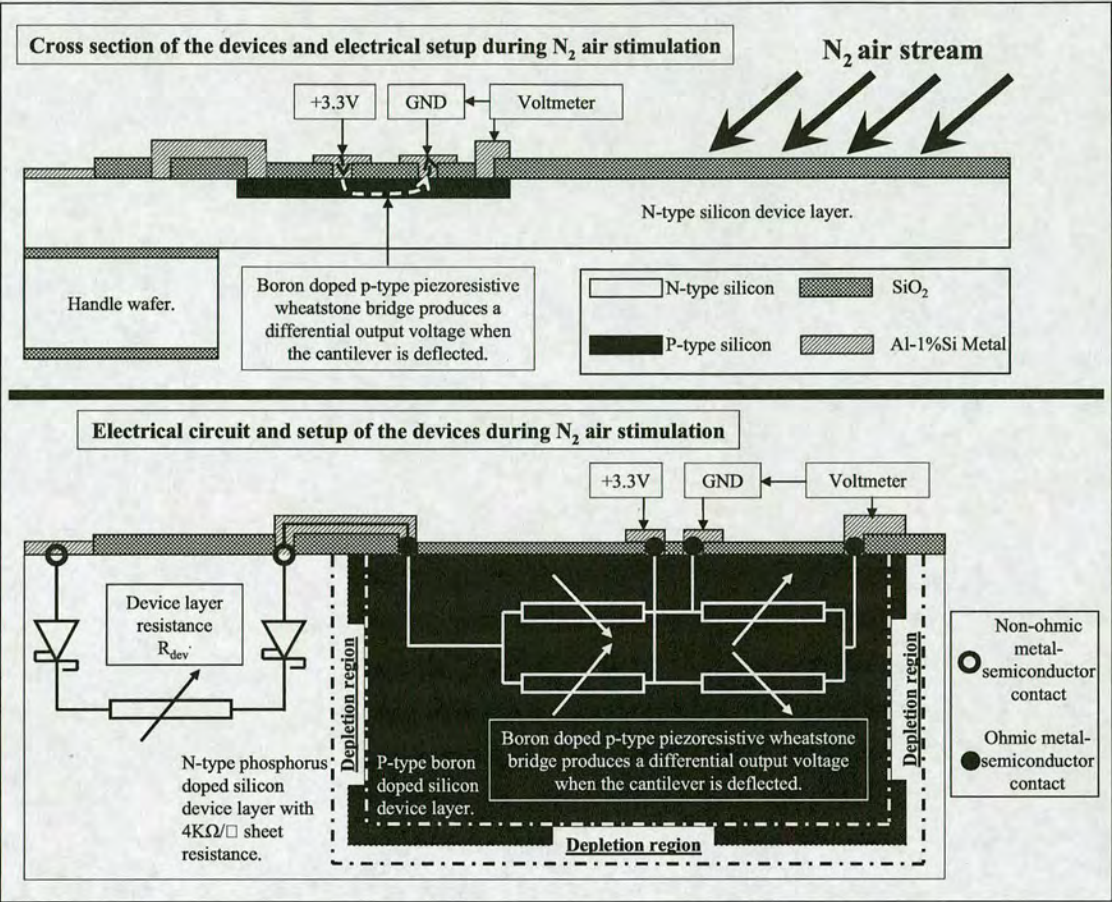
non-linear current-voltage characteristics have been obtained. The specifications in chapter 2, section 2.3 state that the devices should have linear current-voltage characteristics. Since the electrical circuit of the fabricated devices (shown in the lower part of figure 4.8) does not have linear current-voltage properties, it does not meet the specifications.

4.5.3 Probing directly the p-type boron implanted Wheatstone bridge

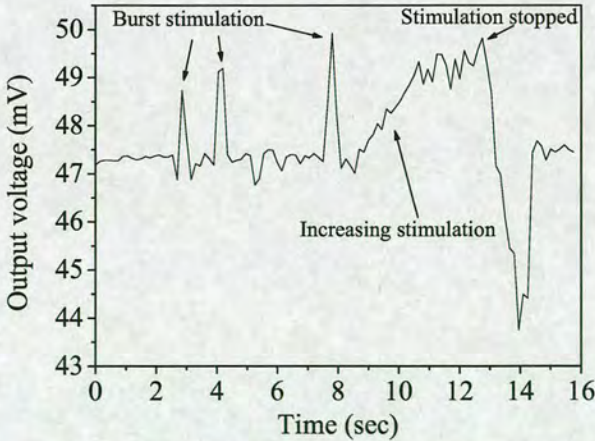
The probing setup in the previous section could not be used to test the performance of the fabricated devices due to the aluminium – n-type semiconductor Schottky barrier. In this section an alternative configuration has been used to test the performance of the device. The three nodes of the p-type boron doped Wheatstone bridge, where the patterned metallisation contacts only the p-type implanted regions, can be probed directly to test the sensitivity performance of strain induced differential output during mechanical deformation of the cantilevers. The probing setup is shown in figure 4.9a where it can be seen that during electrical testing of the $750\mu\text{m}$ long cantilever beam (as shown in the scanning electron micrograph shown in figure 4.6 on page 57 in this section) the n-type device layer has not been used as part of the electrical circuit. The Wheatstone bridge is supplied with power through the two lines that have been designated as the signal output lines, and the signal output is measured at the node that had been designated previously as the Ground line.

The metal – p-type semiconductor contacts have been characterised previously (chapter 3, fig.3.11b, page 45) and have ohmic characteristics, which is ideal for device testing. As can be seen in figure 4.9a, the Wheatstone bridge has been powered at 3.3 volts, N_2 air stream has been applied to the cantilevers and the differential output signal has been recorded. The Wheatstone bridge output signal can be seen in figure 4.9b. The 47mV observed offset voltage of the Wheatstone bridge is within the range of the offset voltage measurements measured previously in chapter 3 (section 3.4.3, figure 3.12a, sub-process A, $2\mu\text{m}$ piezoresistor feature size).

This probing setup has been successfully used to test the device performance. However, because only the three nodes of the wheatstone bridge have been used for this test, a differential output voltage is not available and the device cannot be integrated with the LSI neuron chip. Furthermore, the magnitude of the output voltage of the MEM device has not been adequate for integration with the LSI neuron circuit and a second design iteration that would improve the device sensitivity has been performed and is discussed in chapter 5.



(a) Top part: cross section of the devices, electrical setup and current flow during device testing. Lower part: electrical circuit of the devices and electrical setup during device testing.



(b) The signal output of the probed Wheatstone bridge circuit.

Figure 4.9: a) Electrical configuration during direct probing of p-type Wheatstone bridge, and b) electrical output of Wheatstone bridge integrated with 750μm long cantilever beam, when stimulated with N₂ gun.

4.6 Conclusion

In this chapter the integration of the piezoresistors in Wheatstone bridge configuration with the microcantilever beams has been presented. Initially the p-type boron Wheatstone bridge and the metallisation have been fabricated in section 4.2. Fabrication of the cantilever beams is achieved through patterning of the silicon on insulator wafer device layer to the desired cantilever shape. For the release of cantilevers, the underlying silicon substrate has been etched with bulk micromachining process that removes the silicon of the handle wafer beneath the cantilever beams. The wet TMAH bulk micromachining process described in section 4.3 has been unsuccessful because cracks in the buried oxide layer due to the Si-SiO₂ stress have allowed the etchant to access and etch partly the metallisation and the silicon in the device layer. A solution to overcome the problem of wet etch release has been the use of dry micromachining with deep reactive ion etching in ICP reactor, which has been successfully used to fabricate the microsystems in section 4.4. A final dry etch step has been used to remove the buried silicon oxide layer and release the cantilever beams.

After the successful fabrication of the devices, the electrical tests have been performed to investigate the performance of the devices. As discussed in section 4.5.2, the electrical circuits of the fabricated devices do not have linear current-voltage characteristics and the devices do not meet the specifications.

An alternative setup has been used in section 4.5.3 to probe directly p-type Wheatstone bridge on released silicon cantilever beams in order to test the device performance. The circuit has been found to produce an electrical output when the cantilever beam has been perturbed using a N₂ air stream. However, the devices cannot be integrated with the LSI neuron chip using this probing configuration. Furthermore, the magnitude of the differential output voltage of the tested device has not been found to be adequate for integration with the LSI neuron circuit. A new design approach that would increase the device sensitivity and allow integration with the LSI neuron chip is presented next in chapter 5.

Chapter 5

Second design iteration: integration of half-active Wheatstone bridge circuits with second generation cantilever beams

The MEM system fabricated in this project consists of: a) Wheatstone bridge circuits made of a patterned metallisation and p-type boron doped microfeatures implanted in n-type single crystalline silicon, b) silicon cantilever beams that are integrated with the full-active Wheatstone bridge circuits, and c) out of plane flaps that are integrated at the free end of silicon cantilever beams.

The piezoresistive Wheatstone bridge circuits consisting of p-type boron doped regions implanted in n-type single crystalline silicon, integrated with patterned metallisation have been developed in chapter 3. The first attempt to integrate full-active piezoresistive Wheatstone bridge circuits with released micromachined cantilever beams has been discussed in chapter 4. Although the Wheatstone bridge circuits have produced differential output signal during perturbation of the released cantilever beams, the MEM device did not meet the specifications and could not be integrated with the neuron chip for the reasons discussed in chapter 4. The device is re-designed in this chapter to meet the specifications and allow its integration with the neuron circuit and robot.

5.1 New design considerations

To meet the specifications and allow integration with the LSI neuron circuit and the robot, the MEM devices have been re-designed in this chapter to address the following topics: i) to achieve linear circuit current-voltage characteristics, ii) to improve sensitivity to air stimulation, and iii) to include 32 artificial hair cells in the final device die. The die will be assembled and

bonded in pin grid array (PGA) package, and next it will be installed on pre-designed printed circuit board (PCB) to be electrically interfaced to the LSI circuit/robot system.

5.1.1 Achieving linear current-voltage characteristics

To achieve linear current-voltage characteristics in the new design, each of the 4 nodes of the Wheatstone bridge circuit is integrated with dedicated metal line and bonding pad. The reason for using the 4 node design is that probing directly the p-type piezoresistive Wheatstone bridge with metallic electrodes has been successfully demonstrated in chapter 4, section 4.5.3 to detect the differential output signal of the Wheatstone bridge/aluminium electrodes circuits integrated with released microcantilever beams.

5.1.2 Improving sensitivity to air stimulation

The MEM devices implement p-type piezoresistive strain gauges that are integrated with released micromachined silicon cantilever beams. When a piezoresistor with resistance R is subject to strain ε resulting from lateral out of place movement of the cantilever beam, fractional resistance change ΔR appears in the bulk resistance R , due to the piezoresistive effect. This effect has been demonstrated in chapter 4, section 4.5.3, where p-type piezoresistive Wheatstone bridge circuits integrated with released silicon cantilever beams produced differential output signal when released beams have been perturbed mechanically. The relationship between applied strain ε , piezoresistive bulk resistance R and fractional change ΔR in the piezoresistance is given by the gauge factor K and is defined as $K = \frac{1}{\varepsilon} \frac{\Delta R}{R} \Leftrightarrow \Delta R = \varepsilon(KR)$. From this relationship, for a given gauge factor K and a bulk resistance R , the strain induced fractional resistance change ΔR is proportional to the applied strain ε . Therefore, to achieve maximum fractional change ΔR in piezoresistance, the strain ε applied to the piezoresistors should also be maximized. One method used to improve the strain across piezoresistors is the inclusion of stress concentration regions in the cantilever beams, discussed earlier in the thesis (see Ch.2, sec.2.2.6, pp.21).

In the devices fabricated in the first design iteration in chapter 4, stress concentration regions have been included in the cantilever beams and the p-type boron doped full-active Wheatstone bridges have been positioned in the stress concentration regions. That design is illustrated in figure 5.1a, where the normalized output of the implemented full-active Wheatstone circuit with

four active arms is 1, and the stress concentration factor is equal to $SCF = \frac{b}{a} = \frac{300}{135} = 2.22$. In that design it had not been possible to increase further the stress concentration factor by reduction of the width in the stress concentration region, because the width is essentially limited by the large footprint of the full-active Wheatstone bridge.

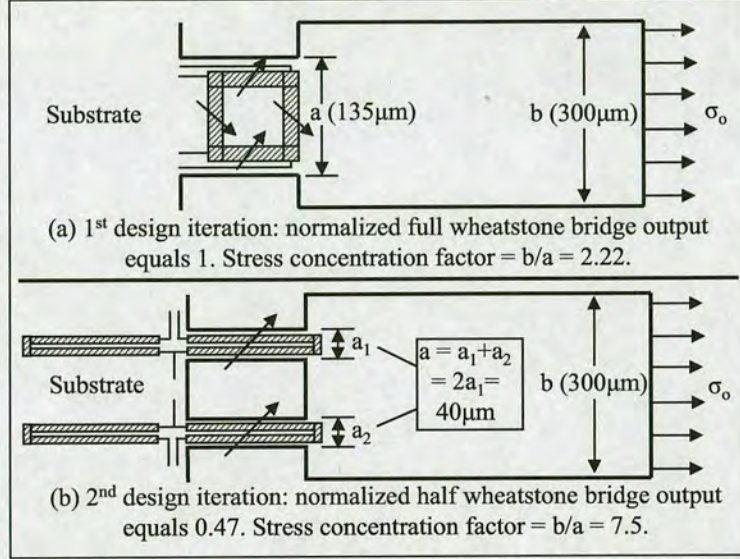


Figure 5.1: Cantilever layout and a) a full-active Wheatstone bridge design from first process iteration, b) a half-active Wheatstone bridge design in second process iteration.

In the second design iteration half-active Wheatstone bridge circuits with normalized output of 0.47 are implemented. The circuit has been designed to accommodate two strain gauges operating in longitudinal mode along the main axis of the cantilever beams and two fixed resistors on the substrate, as seen in figure 5.1b. The advantage of a half-active Wheatstone bridge circuit is its reduced footprint implying that it occupies less space on the stress concentration region of the cantilever beam, making possible further reduction in the width of the stress concentration regions. This improves the stress concentration factor, now calculated to be $SCF' = \frac{b}{2a_1} = \frac{300}{40} = 7.5$, which is larger compared to previous $SCF = 2.22$ for the full-active Wheatstone bridge circuit designed in the first iteration. This implies that for given out of plane deflection of the cantilever beam the applied strain along the strain gauges, hence the fractional change in piezoresistance ΔR should be $\frac{SCF'}{SCF} = \frac{7.5}{2.2} = 3.37$ times larger in the new design compared to the design in the first iteration.

However, the device sensitivity expressed as fractional change in the differential output voltage ΔV of the Wheatstone bridge circuits, is the product of the stress concentration factor and

the normalized Wheatstone bridge output. Table 5.1 lists the sensitivity characteristics of the devices in the 1st iteration and the improved sensitivity characteristics of the devices in the 2nd iteration.

Type	1 st Design Iteration		2 nd Design Iteration
Stress Concentration Factor (SCF)	2.22	<	7.5
Normalized Wheatstone bridge output	1	>	0.47
Calculated device sensitivity	$2.22 \times 1 =$ 2.22	<	$7.5 \times 0.47 =$ 3.525

Table 5.1: *Calculated sensitivities as function of SCF and normalized Wheatstone bridge output.*

5.1.3 Determining the device and metallisation layout

The metallisation configuration and the number of artificial hair cells -consisting of cantilever beams and half-active Wheatstone bridge circuits- per device determine the number of bonding pads on the final device and subsequently the package type/size used to assemble the MEM sensor. Since the number of AHCs has been specified to be 32 per device, the metallisation configuration will ultimately determine the overall number of bonding pads. Next we examine the possible metallisation configurations.

2 bonding pads are required for the differential output signal of each half-active Wheatstone bridge. Power (+V, Ground) lines can be assigned to each Wheatstone bridge using single metallisation layer. However, this approach requires 4 additional power lines/bonding pads per Wheatstone bridge, bringing the total number of bond pads per Wheatstone bridge to $2 + 4 = 6$ and $6 \times 32 = 192$ bonding pads per device. These pads would be bonded on pin grid array (PGA) package measuring 4cm^2 square and the PGA package would be installed on pre-designed printed circuit board (PCB), where the packaged MEM sensor is electrically interfaced to the LSI circuit/robot system. The physical layout of the system can be seen in figure 5.2.

Level 1 is occupied by the robot, that includes integrated circuits, a battery power supply and electrical motors that drive the wheels of the robot. Using metallic pins as support and electrical interconnects, a second PCB is installed on level 2 to accommodate the LSI circuit and a third PCB accommodates the MEM sensor on level 3. As can be seen on the right part of figure 5.2,

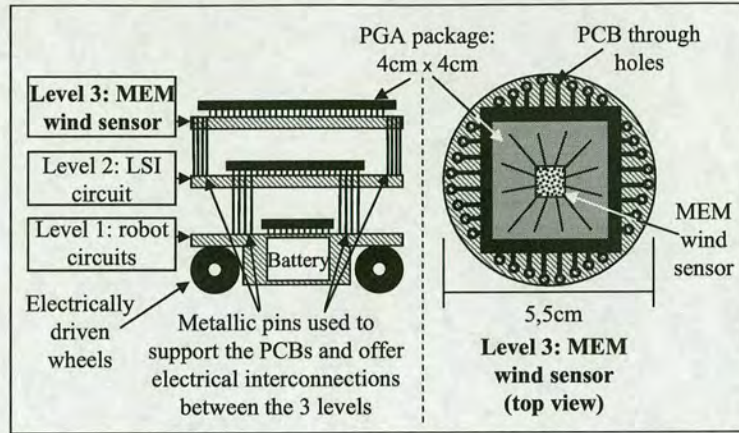


Figure 5.2: Diagram of the MEM air sensor - LSI neuron circuit and robot.

the space available on the PCB is limited and would not have been possible to route 192 lines on the PCB.

The number of metallic lines on the PCB can be limited by reducing the number of bond pads per device die. This can be achieved by implementing multilevel metallisations where each Wheatstone bridge circuit maintains 2 dedicated bonding pads for the differential output signal, but power (+V, Ground) lines are shared by the Wheatstone bridge circuits. The device design that implements multilevel metallisation requires 72 bonding pads (in contrast to 192 bonding pads for the device design with single metallisation) and can be seen in figure 5.3. In this design the length of 32 cantilever beams ranges from $550\mu\text{m}$ to $1250\mu\text{m}$, the width has been constant at $300\mu\text{m}$ and the combined width of the two stress concentration regions has been $40\mu\text{m}$. The cantilevers have been arranged in four arrays in order to provide directional wind sensing after the completion of the fabrication process, including integration of out of plane flaps at the free end of cantilever beams. Similar to the first design iteration, the cantilevers are defined by dry etch of the SOI device layer. For the release of each cantilever beam by dry deep reactive ion etching, individual windows are defined for each cantilever beam on the backside of the wafer. In the lower part of the figure where the magnified view of $550\mu\text{m}$ long cantilever beam has been drawn, the detailed arrangement of the strain gauges, resistors, metallisations, metal – silicon contacts and vias can be seen.

One disadvantage of using multilevel metallisations to reduce the number of device bond pads is that additional SiO_2 dielectric must be deposited on the substrate and between the two metal layers. The side-effect in increasing the total thickness of the dielectric layer is that the boron doped strain gauges, which optimally should be as close to the surface of the cantilevers as

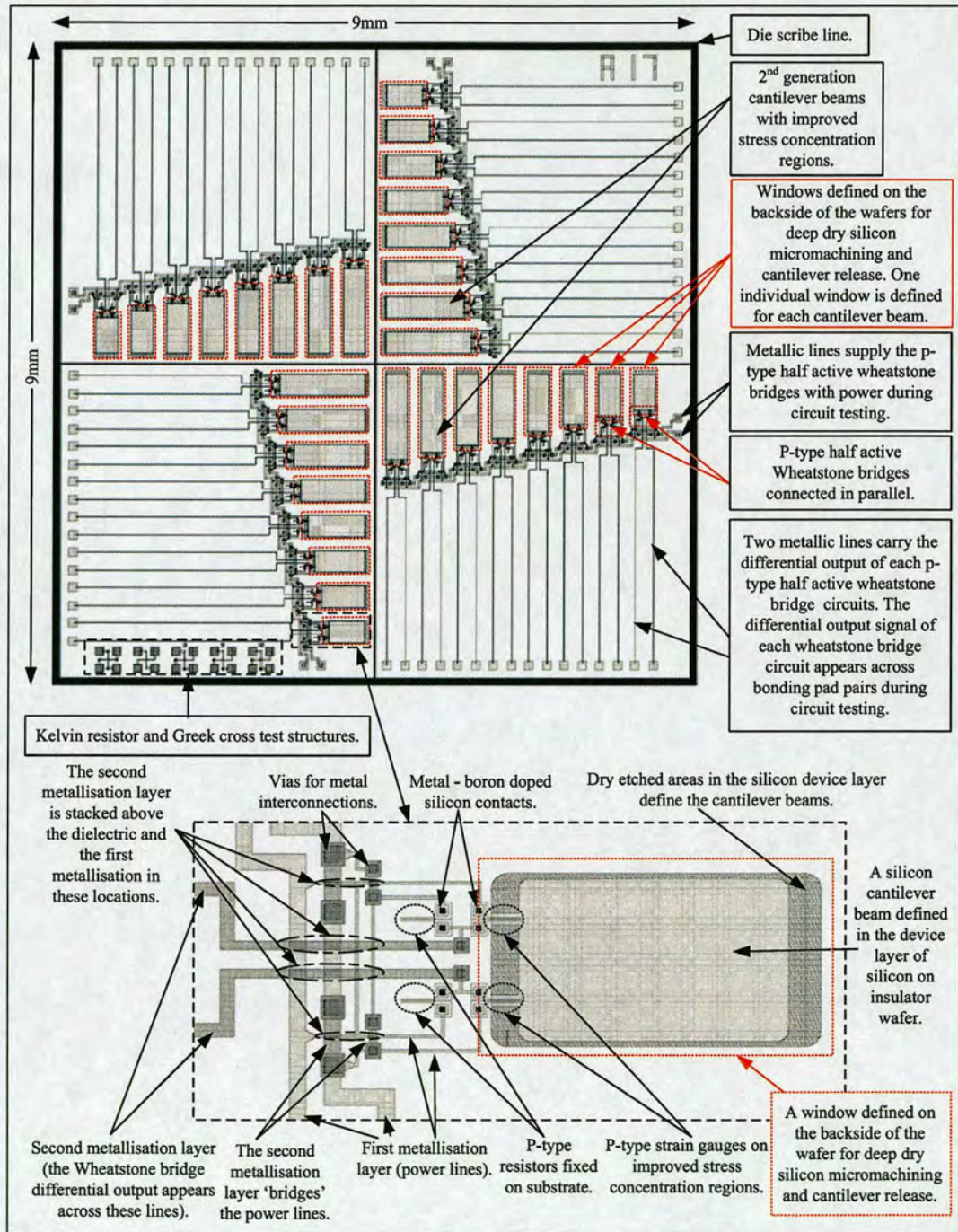


Figure 5.3: Field layout of the MEM devices in the second iteration.

possible where maximum strain appears, now are buried deeper into the body of cantilever beams, which is not optimal. This implies that in the new design the advantage gained by the improved stress concentration regions is partly offset by the reduction in strain gauge sensitivity due to the aforementioned increase in the dielectric thickness on top of the cantilever beams.

The main new feature in the design iteration developed in this chapter is the multilevel metallisations. Before proceeding to the fabrication of the devices on silicon on insulator wafers, the multilevel metallisation process is separately developed next in section 5.2.

5.2 Development of multilevel metallisations with surface planarisation

Because the fabrication of multilevel metallisations is a new process, it has been performed initially on blank silicon wafers, using the process shown in figure 5.4. The process begins with the deposition of a PECVD SiO_2 layer on silicon substrate (fig.5.4a), followed by magnetron sputter deposition, pattern and wet etch of aluminium-one percent silicon alloy (fig.5.4b). Next a 500nm thin PECVD SiO_2 layer is deposited (fig.5.4c) on top of the patterned metallisation to act as dielectric. The profile of two patterned $120\mu\text{m}$ wide metallic bond pads with $0.5\mu\text{m}$ PECVD SiO_2 obtained by a dektak profilometer at this stage of the process can be seen in figure 5.5a.

The PECVD SiO_2 dielectric exhibits poor sidewall profile at the location of the steps defined by the first metallisation, indicated by dashed circles in figure 5.4c. For this reason, the surface of the dielectric must be planarised prior to definition of the vias and deposition of the second metallisation layer. Planarisation here is achieved by spin coating Honeywell accuglass 512B spin-on-glass (SOG) layer on the surface of the substrate, followed by thermal curing of the SOG. This material contains 15wt% CH_3 (methyl) groups bonded to Si atoms in the Si-O backbone and exhibits low shrinkage during the thermal curing process [55].

The SOG has been spun-coated on the substrate and it has been stabilized using a thermal curing process (fig.5.4d). To thermally cure the SOG, the wafers have been loaded in oven at room temperature and the temperature has been ramped at $4^\circ\text{C}/\text{min}$ up to 200°C , it has been maintained at this level for 30 minutes, and finally it has been ramped down at $4^\circ\text{C}/\text{min}$ to room temperature. After the low temperature process the spin-on-glass has been partly cured.

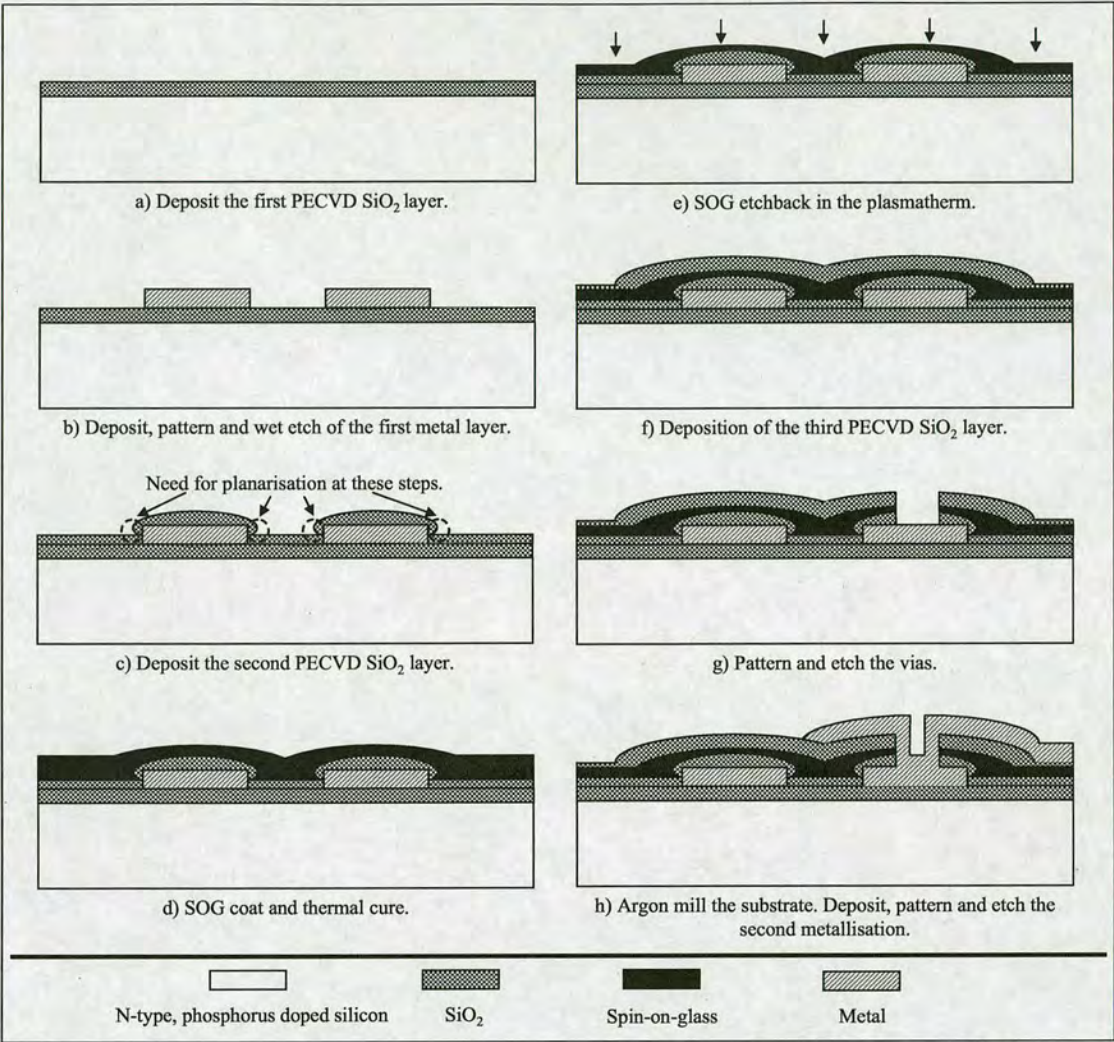


Figure 5.4: The multilevel metallisation process including planarisation of the substrate's surface.

To complete the curing process, the wafers have been sintered at 435°C in N₂/H₂ forming gas for 15 minutes. The sinter step is required to complete the molecular bonding processes and curing of the spin-on-glass thin film [56] in order to prepare the substrate for the etch back step. Profilometry results obtained by a dektak at this stage of the process are shown in figure 5.5b, where it is observed that the spin-on-glass has effectively smoothed the sidewall profiles and the step of the metallic bumps has been reduced by 0.09µm, from 0.5µm to 0.41µm.

After the sinter step, optical inspection of the substrates has revealed hillock formation on aluminium lines. This is a known issue and is due to the low melting point and recrystallization of aluminium metallisation after the sinter step [57, 58]. Although anodization of aluminium

film in boiling de-ionized water at 80°C has shown to reduce the amount of hillock formation, this step has not been performed here. However, these hillocks have not been detected by dektak profilometry at this stage of the process, as can be seen in figure 5.5b, because the thermally cured spin-on-glass has planarized the hillocked surface of the aluminium metallisation.

The samples have been diced and the thickness of the deposited spin-on-glass has been investigated in the scanning electron microscope. The thickness has been determined to be approximately 0.85µm thick on top of the metal lines and has been slightly thicker at approximately 1µm elsewhere. After spin coating and thermal curing, the spin-on-glass thin film is thicker than required for the planarisation purpose. A dry etch back step in CF₄/H₂ plasma can be used to reduce the thickness of the film, while maintaining the planarized property of the substrate surface.

5.2.0.1 Characterisation of the spin-on-glass etch back

The spin-on-glass etch rate in CF₄/H₂ plasma in the Plasmatherm reactive ion etch tool has been found to be 42nm/min versus 25nm/min (17nm/min differential etch rate) for the PECVD SiO₂. Next, to determine the optimum etch back time for the planarized substrates, several etch steps have been performed and the surface profile has been investigated with dektak profilometer after each etch step.

The profile of metallic pads after coating with spin-on-glass and before the etch back steps can be seen in figure 5.5b. After a 5 minute etch back step in CF₄/H₂ plasma the profiles can be seen in figure 5.5c where significant alteration in the profiles of the bumps has not been observed. Etching back for additional 10 minutes (15 minute cumulative etch time) reduces the thickness of the spin-on-glass further and the etch front approaches the first PECVD SiO₂ layer, revealing the surface roughness from the aluminium hillocks. As mentioned previously, the hillocks on top of the aluminium have been formed during the sinter step at 435°C. The step height of planarized bumps at this stage of the etch back process has not been modified and has remained equal to 0.41µm, as can be seen in figure 5.5d.

A final etch back step for additional 10 minutes (25 minutes cumulative etch time) has been performed and profilometry measurements are illustrated in figure 5.5e. The roughness on the surface of the bumps due to aforementioned aluminium hillocks is also visible here. Furthermore, it is observed that the height of planarized bump step has been increased from 0.41µm

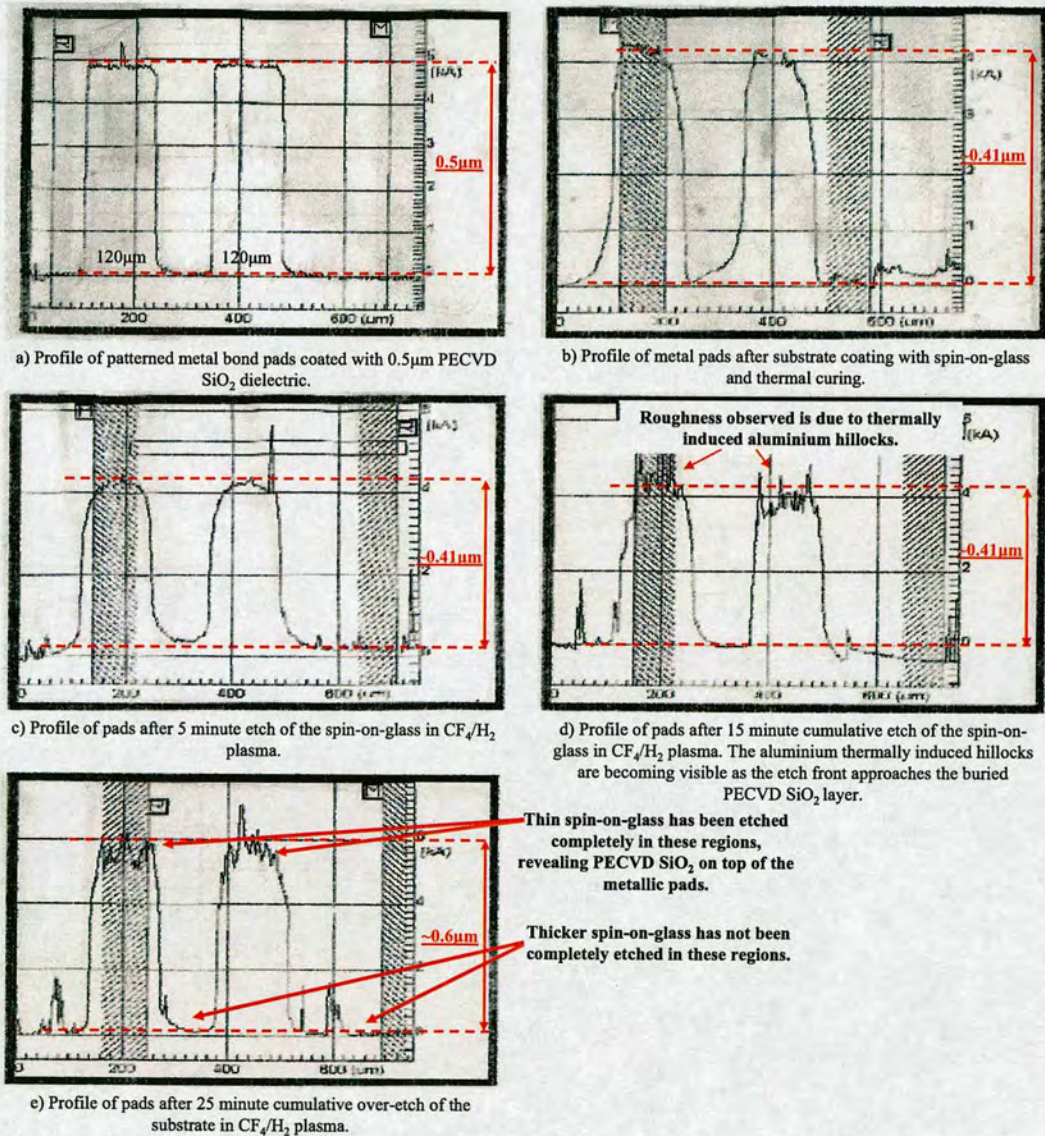


Figure 5.5: Evolution of metal bump profiles during the substrate surface planarisation process with spin-on-glass.

0.6 μ m. This indicates that the spin-on-glass on top of the bumps has been completely removed, revealing the PECVD SiO₂. Because the revealed PECVD SiO₂ on top of the bumps is etched slower compared to the remaining spin-on-glass on the surface of the substrate, the profiled step height increases as the remaining spin-on-glass on the substrate is being etched at faster rate [compared to PECVD SiO₂ on top of the bumps]. At this stage the substrate has been over-etched and as this is not desirable, the cumulative etch back time should not exceed 15 minutes.

After investigation of the etch back process, the remaining wafers subsequently have been etched for 15 minutes, removing approximately 630nm of cured spin-on-glass (step shown in fig.5.4e). Next, the third 500nm thin PECVD SiO₂ layer has been deposited (fig.5.4f) and the wafers have been patterned photolithographically to define the vias. The stacked dielectric layers (PECVD SiO₂-SOG-PECVD SiO₂) have been dry etched in CF₄/H₂ plasma to define the vias (fig.5.4g), expose the underlying metal and prepare the substrates for deposition of the second metallisation layer.

5.2.0.2 Deposition and definition of the second metallisation

Prior to depositing the second metal layer, the surface of the substrate is cleaned by milling with ionic argon for 20 minutes. This is a standard procedure in multilevel metallisation processes. Immediately after the argon mill, 0.5 μ m pure aluminium has been deposited by magnetron sputtering. Next the wafers have been patterned photolithographically and wet etched to define the second metallisation. After stripping the remaining photoresist in O₂ plasma, an additional sinter step at 435°C in H₂/N₂ environment for 15 minutes (bringing the total sinter time to 30 minutes) has been performed. After the completion of the process, samples have been inspected in the scanning electron microscope. The micrograph in figure 5.6 shows that after the dielectric planarisation process the continuity of 5 μ m narrow metal lines is maintained even after wet etching of the samples.

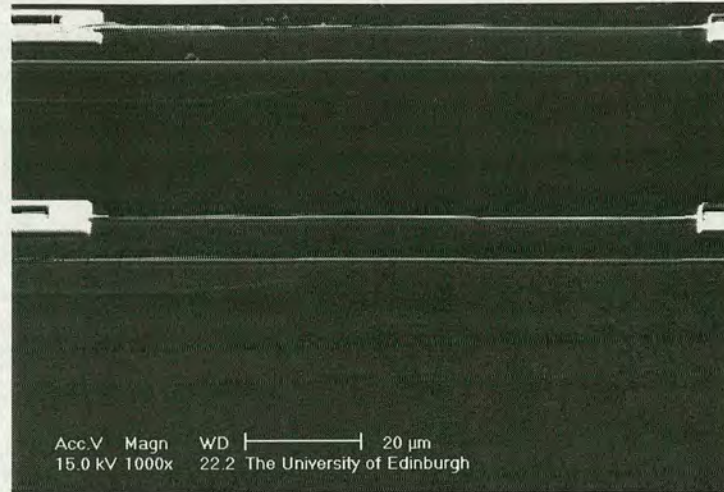


Figure 5.6: *Multilevel metallisations with a planarized dielectric surface. The continuity of the second metallisation layer is maintained on top of the planarised bumps, which are defined by the first metallisation.*

5.3 Device fabrication

After the development of the multilevel metallisation process in section 5.2, the MEM devices that include half-active Wheatstone bridge microfeatures and a two-level metallisation, are integrated with second generation silicon cantilever beams using the fabrication process shown in figure 5.7. Starting with silicon on insulator wafer (fig.5.7a), a $0.5\mu\text{m}$ thin PECVD SiO_2 implantation mask has been deposited, photolithographically patterned and etched in a CF_4/H_2 plasma to define the implantation windows (fig.5.7b). The substrates have been implanted with boron at 30keV, 55keV and 80keV energies and dose 3.5×10^{13} atoms/ cm^2 to define the piezoresistors (fig.5.7c), followed by boron activation at 1000°C for 35 minutes in N_2 environment. The implantation mask has been stripped in hydrofluoric acid (fig.5.7d) and a $0.5\mu\text{m}$ thin PECVD SiO_2 passivation has been deposited on the substrates (fig.5.7e). Next the metal – semiconductor contact windows have been defined with photolithography and a subsequent dry etch step in the CF_4/H_2 plasma removed selectively the PECVD SiO_2 dielectric. The first, $0.5\mu\text{m}$ thin aluminium-1% silicon metallisation layer has been deposited on the substrate and has been defined with photolithography and heated wet etchant (fig.5.7g). An additional $0.5\mu\text{m}$ thin PECVD SiO_2 layer has been deposited on the substrates (fig.5.7h), followed by planarisation with spin-on-glass (fig.5.7i), sintering at 435°C for 15 minutes in N_2/H_2 environment and etch back of the spin-on-glass in the CF_4/H_2 plasma for 15 minutes. The final PECVD SiO_2 layer, $0.5\mu\text{m}$ thin has been deposited (fig.5.7j) and the vias have been defined on the substrate

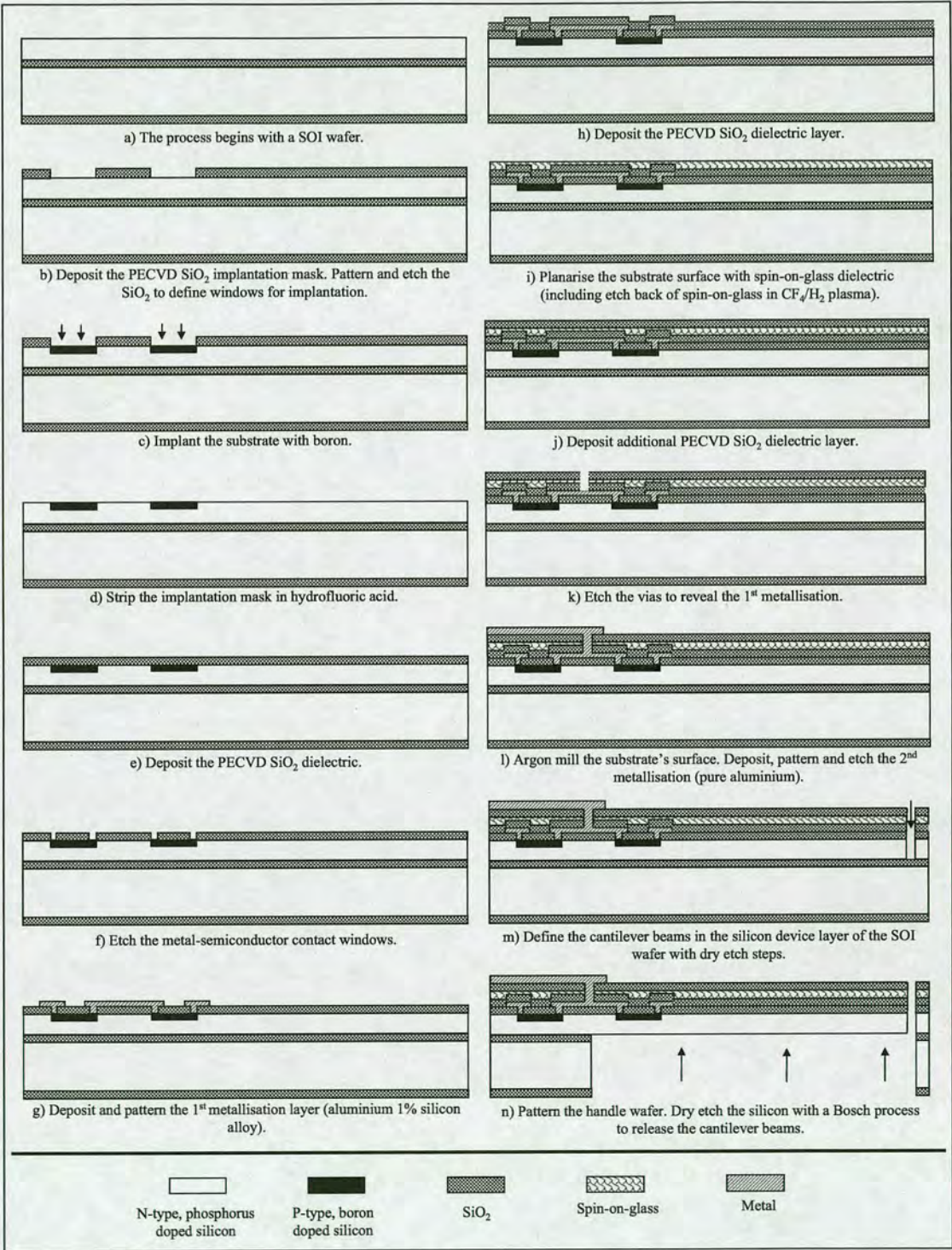


Figure 5.7: Fabrication process for half-active Wheatstone bridge circuits, integrated with metallisation in two levels and released silicon microcantilever beams.

with photolithography and dry etch of the SiO_2 dielectric in the CF_4/H_2 plasma (fig.5.7k). The wafers have been milled with argon for 20 minutes in the Balzers tool and the second metallisation, $0.5\mu\text{m}$ of pure aluminium, has been deposited and patterned with photolithography and wet etch (fig.5.7l). A second sinter step at 435°C for 15 minutes in N_2/H_2 environment, bringing the total sinter time to 30 minutes, has been performed to improve the metal – semiconductor contacts and metal – metal contacts.

After the fabrication of circuits (p-type Wheatstone bridges/two-level metallisation), the silicon device layer has been patterned photolithographically to define the cantilever beams. In the first design iteration $7\mu\text{m}$ thick photoresist has been used for this step, but now $1.35\mu\text{m}$ thin photoresist has been implemented. Reduction in the thickness of the resist (see equation 3.3, pp.37), would lead to improved printing resolution, hence sharper reproduction of the feature corners and smaller fillet radii at the stress concentration regions. This leads to improved stress concentration factor and improved device sensitivity (see Ch.2, sec.2.2.5, pp.20). After the lithographic step the cantilevers have been defined by dry etching of the silicon device layer in ICP reactor using Bosch recipe ‘A’ (fig.5.7m - Bosch work conditions can be found in table B.3, appendix B). Finally the cantilevers have been released by dry etch of the handle wafer in ICP reactor using Bosch recipe ‘A’ and dry etch of the buried SiO_2 beneath the cantilever beams in CF_4/H_2 plasma (fig.5.7n).

A photograph of a wafer after the fabrication process can be seen in figure 5.8 and details of fabricated devices can be found in table 5.2 on the next page. Next, the wafers have been diced to inspect and test the devices.

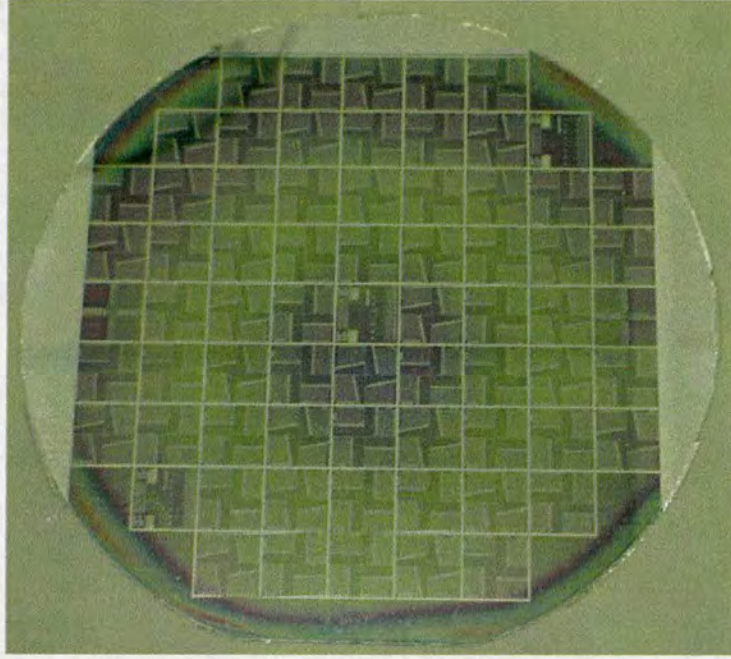


Figure 5.8: Photograph of fabricated devices on wafer. The observed metallic scribe lines define 63 die on the wafer. The circumferential colored rings indicate a smooth variation in the thickness of the deposited film. This has been caused by standing waves formed during the spin-on-glass spin coating process.

Type	Thickness (μm)	Dopant	Sheet Resistance (Ω/\square)	Function
Aluminium	0.5	-	Not measured	Level 2 metallisation
SiO ₂ layer 3	0.5	-	-	Dielectric
Spin-on-glass	0.2	-	-	Dielectric / surface planarisation
SiO ₂ layer 2	0.5	-	-	Dielectric
Aluminium 1% silicon	0.5	-	62×10^{-3}	Level 1 metallisation
SiO ₂ layer 1	0.5	-	-	Dielectric
Resistors/ Strain Gauges	~ 0.5	Boron	1307 (30KeV*) 1145 (55KeV*) 1092 (80keV*)	Half-active Wheatstone bridge
Silicon device layer	15	Phosphorus	4000	Cantilever beams
Buried SiO ₂	2	-	-	Etch stop layer
Silicon handle wafer	425	Phosphorus	Not measured	Support

* Boron has been implanted at 3.5×10^{13} atoms/cm² dose.

Table 5.2: Details and function of each layer in the fabricated MEM devices.

5.4 Device testing and troubleshooting

After dicing the wafers to individual die, the devices have initially been inspected in the optical microscope. High magnification optical micrographs of a fabricated microcantilever beam integrated with the electrical circuit (Wheatstone bridge/metallisations) are shown in figure 5.9.

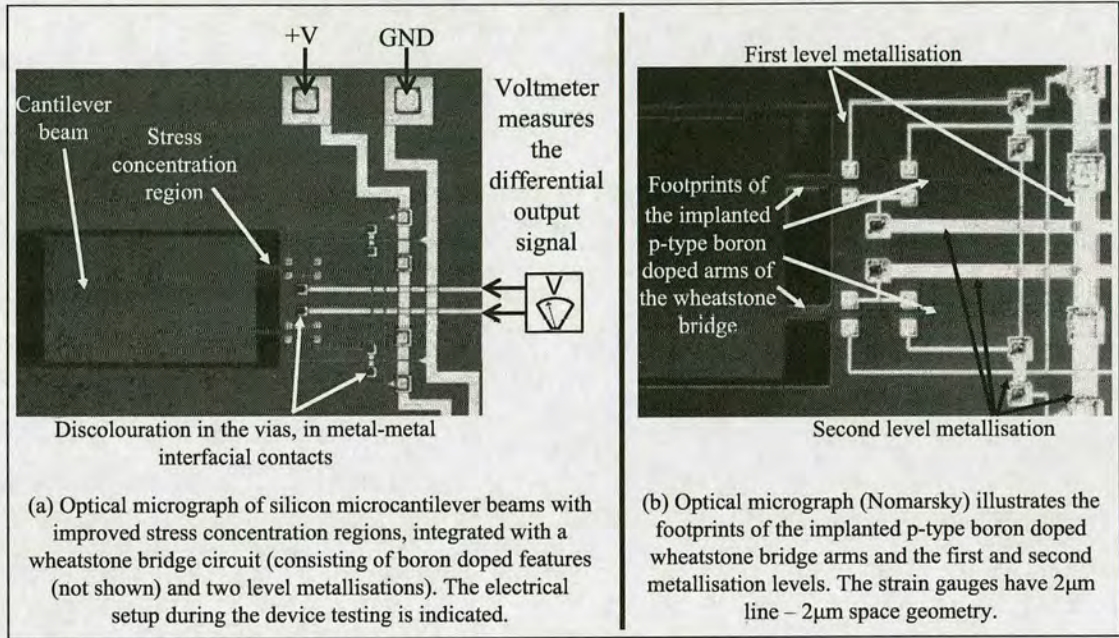


Figure 5.9: High magnification optical micrographs of a fabricated cantilever beam, integrated with a half-active Wheatstone bridge and a two-level metallisation.

Discoloration is observed at the location of the vias, where the second metallisation (pure aluminium) has been deposited on top of the first metallisation (aluminium-1% silicon). This indicates that diffusion takes place between the two metal layers at the vias. This would have been avoided if titanium diffusion barrier layer has been deposited as part of the second metallisation, prior to depositing the pure aluminium metal layer.

To test the performance of the fabricated devices, these have been probed using the configuration shown in figure 5.9a. However, when voltage has been applied across the power lines, electrical current could not flow through the circuit implying electrical discontinuity at some point in the circuit. Additional inspection of devices in the scanning electron microscope has indicated failure of the second metallisation layer at the Via sidewalls, as shown in figure 5.10. This is likely to have been due to poor adhesion of aluminium on the dielectric sidewalls and subsequent delamination off the sidewalls during sinter step. A first step to improve this would

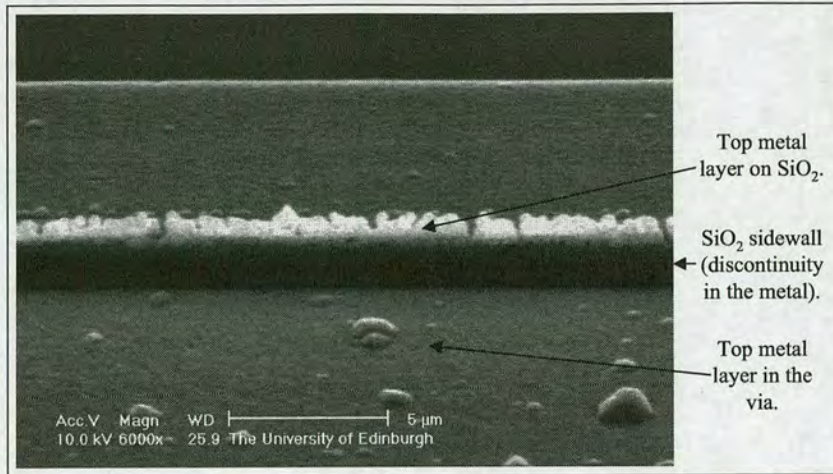


Figure 5.10: SEM micrograph indicates the discontinuity of the metal on a via sidewall.

be the deposition of titanium layer as part of the second metallisation. The titanium layer would act as a diffusion barrier between the two metallisations at the location of the vias and as an adhesion layer for the pure aluminium layer of the second metallisation layer.

5.5 Conclusion

To meet the specifications and allow integration with the LSI neuron circuit and the robot, the MEM devices have been re-designed in this chapter to address the following topics: i) to achieve linear circuit current-voltage characteristics, ii) to improve sensitivity to air stimulation, and iii) to include 32 artificial hair cells in the final device die. The device die would be assembled and bonded in PGA package, and would be installed on pre-designed PCB, where it would be electrically interfaced to the LSI circuit/robot system.

In section 5.1 the new device design has been presented. The re-designed devices feature half-active Wheatstone bridge circuits for integration with second generation microcantilever beams that include improved stress concentration regions and improved sensitivity to air stimulation.

In order to allow integration of the MEM device that includes 32 AHCs with the LSI circuit and robot in printed circuit board with limited surface area, as seen in figure 5.2, the electrical line paths on the PCB should be minimized, hence so should the number of bonding pads on the MEM device. For this reason, multilevel metallisations in two levels have been implemented, where the power (+V, Ground) lines are shared by Wheatstone bridge circuits

The two-level metallisation process that includes surface planarisation of the SiO_2 dielectric has been developed in section 5.2. Finally the new MEM devices that include half-active Wheatstone bridge circuits integrated with a two-level metallisation and second generation silicon micromachined cantilever beams have been fabricated in section 5.3.

The devices have been tested in section 5.4 and have been found to be non-conducting, implying electrical discontinuity at some point in the electrical circuit. The devices have been troubleshot both electrically and in scanning electron microscope, where failure of the second metallisation layer due to poor adhesion of aluminium at the sidewalls of the vias has been confirmed. Future work would include deposition of titanium adhesion layer as part of the second metallisation (prior to deposition of pure aluminium layer) in order to resolve the aforementioned issue.

Chapter 6

Plastic deformation magnetic assembly (PDMA)

The MEM system fabricated in this project consists of: a) Wheatstone bridge circuits made of a patterned metallisation and p-type boron doped microfeatures implanted in n-type single crystalline silicon, b) silicon cantilever beams that are integrated with the full-active Wheatstone bridge circuits, and c) out of plane flaps that are integrated at the free end of silicon cantilever beams.

The piezoresistive Wheatstone bridge circuits consisting of p-type boron doped regions implanted in n-type single crystalline silicon, integrated with patterned metallisation have been developed in chapter 3. Initially the integration of full-active Wheatstone bridge circuits consisting of four active arms and single layered metallisation with micromachined silicon cantilever beams has been attempted in chapter 4, but the fabricated devices did not have linear ohmic current-voltage electrical characteristics. The device design has been re-iterated in chapter 5, where the integration of half-active Wheatstone bridge circuits (2 active piezoresistive arms / 2 fixed resistors and metallisation in two levels) with the micromachined silicon cantilever beams has been attempted.

In order to produce out of plane flaps of variable length that transfer air-induced torque to released cantilever beams, the plastic deformation magnetic assembly for integration of out of plane flaps at the free end of silicon cantilevers is developed. The drag that acts across the flaps when wind moves would cause a torque to appear across the cantilevers, resulting in a mechanical deformation. The mechanical deformation would be detected by the piezoresistive p-type Wheatstone bridge circuits, which are integrated with the cantilever beams.

Due to the complexity of the plastic deformation magnetic assembly process, it has been developed initially on trial three inch wafers prior to its integration with micromachined silicon cantilever beams. The plastic deformation magnetic assembly process development is presented in the next sections.

6.1 Fabrication steps

To achieve out of plane flaps as the final structures, a metallic seed layer is deposited on a sacrificial layer and nickel-iron permalloy is electrodeposited on top of the metallic seed layer. To achieve out of plane deformation of the composite seed layer – Ni-Fe permalloy flaps, the sacrificial layer is removed to release the flaps. The released flaps are exposed to magnetic field and under the influence of magnetic flux, torque appears across the Ni-Fe permalloy causing out of plane deformation of the composite seed layer – Ni-Fe permalloy flaps.

The PDMA fabrication process is shown in figure 6.1. The process starts with the deposition (fig.6.1a), photolithographic pattern and etch (fig.6.1b) of a sacrificial layer, where the etched areas define the anchors of the out of plane flaps. Next, the wafers are patterned photolithographically with resist for lift-off process (fig.6.1c), the metallic seed layer is deposited on the wafers by thermal evaporation or magnetron sputtering (fig.6.1d), and lift-off is performed in ultrasonic bath with photoresist remover (fig.6.1e). Because the structures defined by the metallic seed layer cover large areas, release holes have been included in the design to assist in fast etch of the sacrificial layer. After the lift-off process has been complete, a $15\mu\text{m}$ thick mold is prepared by double coating of SPR220.7 photoresist, which is photolithographically patterned to define the electrodeposition areas (fig.6.1f). Next the nickel-iron film is electroformed on the exposed metallic seed layer (fig.6.1g) and the photoresist mold is removed in acetone followed by isopropanol bath. Finally, depending on the material the sacrificial layer is made of, this is removed by an appropriate dry or wet etch step, and the flaps are released (fig.6.1h). A magnetic field is applied and the torque appears on the electroformed permalloy (fig.6.1i) causing plastic deformation of the seed layer at the location of the hinge (fig.6.1j) and consequently out of plane bending of the structures. Because the seed layer is only $0.5\mu\text{m}$ thick, the hinge is not rigid and the flaps can move freely (even after the completion of the PDMA process) in the presence of wind, without transferring the torque on the main silicon cantilevers. Therefore a suitable technique that would strengthen the hinge and provide structurally rigid flaps must be implemented.

The PDMA process development is divided in three main parts: i) the investigation of working release methods, where a sacrificial layer is combined with a metallic seed layer followed by etch of the sacrificial layer and release of the overlying metallic seed layer, ii) the characterisation of the nickel-iron permalloy electrodeposition on the metallic seed layer, iii) the integration of the sacrificial layer with the metallic seed layer and Ni-Fe permalloy electrodeposited on top

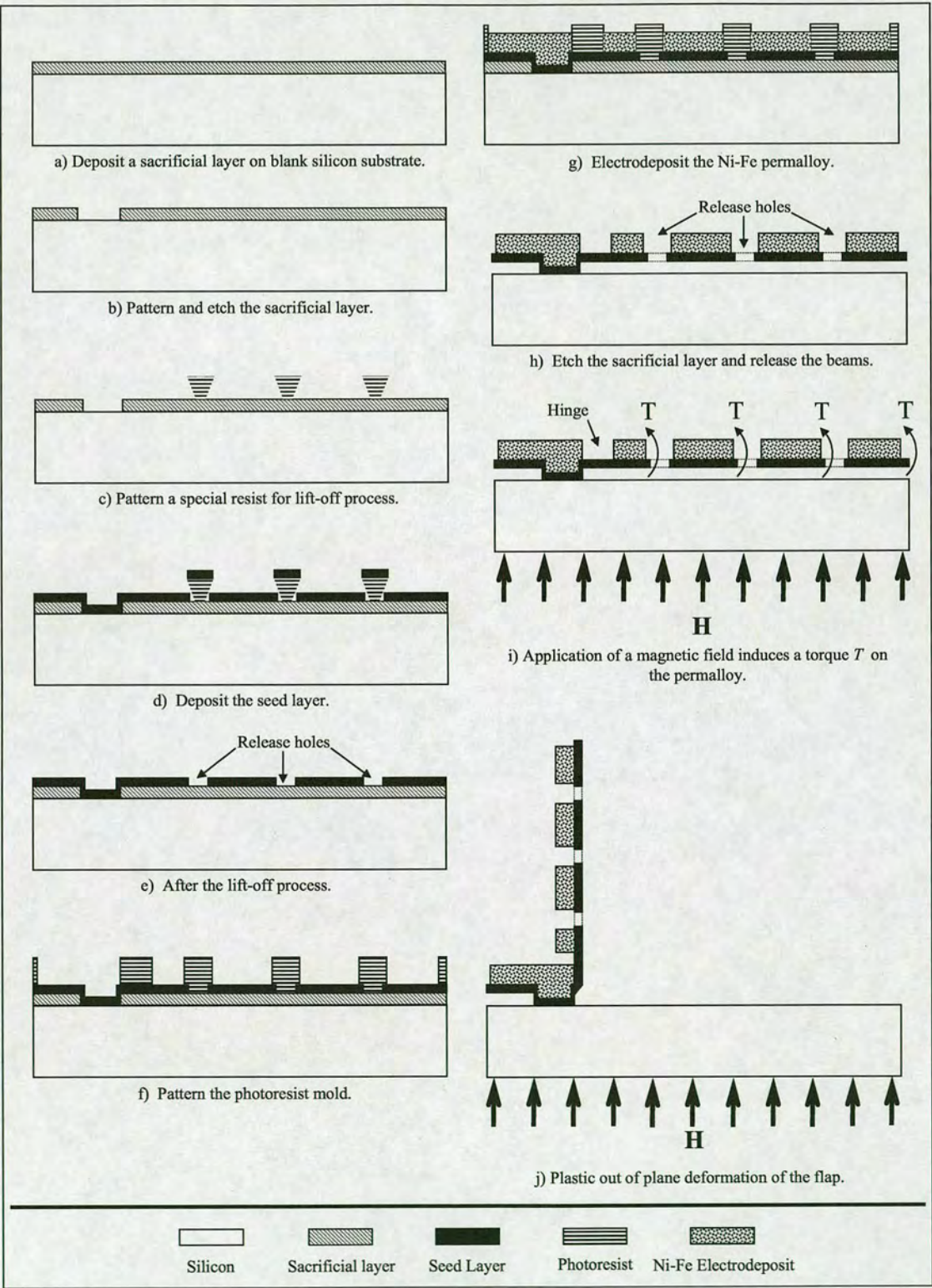


Figure 6.1: Fabrication diagram of the plastic deformation magnetic assembly process.

of the seed layer and etch of the sacrificial layer to release the composite seed layer – Ni-Fe permalloy flaps, followed by deformation of the flaps through exposure to magnetic field.

6.2 Investigation of release methods by sacrificial etch

The first step in developing the PDMA process is the investigation of a working release method, where a sacrificial layer is etched to release an overlying metallic seed layer and electroformed permalloy. The metallic layer is deposited on top of the sacrificial layer and acts as seed for the nickel-iron permalloy electrodeposit. Once the Ni-Fe has been electroformed on the metallic seed layer, the sacrificial layer is etched away to release the composite seed layer – Ni-Fe permalloy flaps. To achieve fast etch of the sacrificial layer and fast release of the structures, release holes have been included in the composite seed layer – Ni-Fe permalloy structures.

The etchant employed for the sacrificial etch step ideally should react with the sacrificial layer only and should not etch any other materials that constitute the MEM device (Si, SiO₂, Al-1%Si metallisation, metallic seed layer, Ni-Fe permalloy). Furthermore, the release etch methods fall in one of the two categories: dry or wet. A dry sacrificial etch/release is always the preferred approach because it is easier to perform, in contrast to a wet etch approach that requires rinsing and drying of the substrates after completion of the release process. In addition, because the released MEM structures are extremely fragile, the rinsing and drying steps that follow a wet etch release step may cause fracture of the released structures and significantly reduce the fabrication yield. This issue is avoided in the dry etch approach because it does not require post-release sample cleaning.

Initially the polyimide sacrificial layer combined with either a nichrome adhesion layer/copper seed layer or a titanium adhesion layer/nickel seed layer have been investigated. Polyimides are organic films that can be dry etched in O₂ plasma, which does not react with any other materials (Si, SiO₂, Al-1%Si metallisation, metallic seed layer, Ni-Fe permalloy) that constitute the devices. Furthermore the dry etch plasma release process is very attractive due to the aforementioned advantages (ease of use, high yield). The main reason for choosing copper and nickel metals is their availability and their suitability to act as seeds for electrodeposition of Ni-Fe permalloy. However due to the poor adhesion of copper or nickel with polyimide, additional adhesion layers (nichrome or titanium) have been deposited between the polyimide sacrificial layer and the metallic seed layers.

The second sacrificial layer employed has been SiO₂ combined with an overlying nickel seed layer. The SiO₂ layer is etched in hydrofluoric acid to release the nickel seed layer. Performing the sacrificial etch and release process in wet hydrofluoric acid solution is less desirable compared to the O₂ plasma dry release approach due to the aforementioned disadvantages of wet microstructure release (not ease of use, low yield due to post-release sample cleaning). Furthermore, during the SiO₂ sacrificial etch and nickel seed layer release process, the hydrofluoric acid would also etch the SiO₂ dielectric in the electrical circuits of the MEM device. Therefore some sort of protective coating would have to be added onto the areas occupied by the electrical circuits to avoid etch of the SiO₂ dielectric.

The different combinations of sacrificial layers, release methods/tools used to etch the sacrificial layers and the seed layers investigated in this phase of the PDMA development process are summarized in table 6.1.

Sacrificial layer	Release Type	Etch chemistry	Tool	Adhesion layer	Seed layer	Electrodeposited Permalloy	Developed in section
Polyimide	Dry	O₂ plasma	Barrel asher	Nichrome	Copper	No	6.2.1.1
			Barrel asher	Titanium	Nickel	No	6.2.1.2
			Remote plasma source	Titanium	Nickel	No	6.2.1.2
SiO₂	Wet	Hydrofluoric acid (buffered)	Bath	-	Nickel	No	6.2.2
	Vapor	Hydrofluoric acid	Memsstar	-	Nickel	Yes	6.4.2

Table 6.1: Summary of the sacrificial layers, adhesion and seed layers and sacrificial etch methods used.

The fabrication details of the PDMA development process starting with the investigation of the polyimide sacrificial layer is described next.

6.2.1 Polyimide sacrificial layer for dry etch in O₂ plasma

A polyimide sacrificial layer to be dry etched in oxygen plasma has been attempted. The overlying metallic seed layer would be released after the complete etch of the underlying polyimide sacrificial layer. Polyimides are polymers that exhibit an exceptional combination of thermal stability, mechanical toughness and chemical resistance. The use of polyimide as sacrificial layer here is highly desirable because it can be etched in O₂ plasma. Since the O₂ plasma does not react with any of the materials (aluminium metallisation, SiO₂ dielectric, silicon) that

constitute the MEM device, it is the most desirable option.

Polyimide PI2545 from DuPont has been used here. The substrate's surface has been treated with a liquid primer and the polymer has been subsequently spun coated at 3000rpm for 60 seconds (fig.6.1a). The ramped temperature process used previously in chapter 5 for the spun coated spin-on-glass, has also been used to cure the spun coated polyimide thin film. After coating with polyimide, the wafers have been loaded in the oven at room temperature oriented horizontally. The temperature has been ramped at 4°C/min up to 200°C and it has been maintained at this temperature level for 30 minutes. Finally the temperature has been ramped down at 4°C/min rate down to room temperature, ending the thermal curing process. After the curing process has been complete, the chemical inertness of the polyimide thin film had been improved and it could not be dissolved in acetone, photoresist remover or photoresist developer. However, fuming nitric acid and O₂ plasma could etch the thermally cured film.

Next, to define the flap anchors the wafers have been patterned photolithographically and the polyimide has been etched in the Plasmatherm, in reactive ion O₂ plasma, using photoresist as a mask (fig.6.1b). After the etch process has been complete, the remaining photoresist has been stripped in photoresist remover and, using a dektak surface profilometer, the thickness of the polyimide film has been determined to be 1.7μm. Deposition of a nichrome adhesion layer and copper seed layer on underlying sacrificial polyimide layer and the attempt to release the seed layer, by etch of the polyimide in O₂ plasma, is described next.

6.2.1.1 Release of thermally evaporated nichrome adhesion layer and copper seed layer deposited on top of the polyimide sacrificial layer

The seed layer is a suitable conducting metal where the nickel-iron permalloy is electrodeposited onto. As can be seen in figure 6.1c-d, photoresist for lift-off is patterned on top of the sacrificial layer to prepare the substrate for the deposition of the metallic seed layer. Next the seed layer is deposited on the substrate and lift-off is performed, leaving the remaining patterned seed layer on the sacrificial layer and the anchor.

Because copper exhibits poor adhesion with the polyimide sacrificial thin film, a 30nm nichrome adhesion layer followed by 500nm copper seed layer have been deposited by the method of thermal evaporation at 1.5×10^{-2} mT work pressure. Furthermore, films deposited by the method of thermal evaporation exhibit poor sidewall coverage (which is desirable in lift-off processes)

and AZ5214E image reversal photoresist with negative sloped sidewall is adequate for lift-off of such metallic thin films. After the evaporation of metallic films and completion of the lift-off process -in resist remover assisted by ultrasonic bath- the samples have been exposed to O_2 plasma in the barrel asher in order to etch the polyimide and release the seed layer.

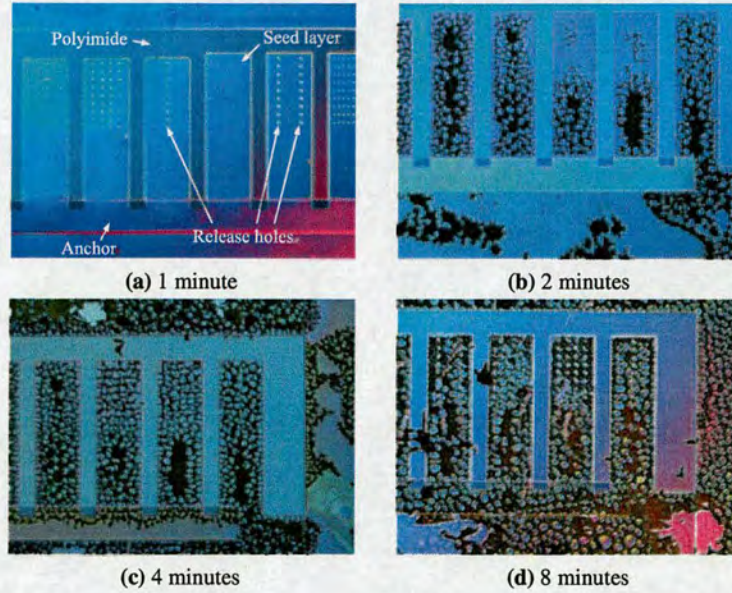


Figure 6.2: Optical microscope images (Nomarski) showing rapid progressive cracking of the thin films after short exposures in O_2 plasma, in the chamber of the Barrel asher. The width of the flaps is $300\mu m$.

Inspection of the samples after short exposures to the plasma revealed severe cracking and failure of the thin films. The optical micrographs (Nomarski) can be seen in figure 6.2. The etch of the polyimide thin film in the images shown has been incomplete and there is still residual polyimide remaining beneath the nichrome adhesion layer/copper seed layer. The failure observed is possibly due to a combination of several factors. One factor is the elevated temperature in the chamber that can reach $140^\circ C$, leading to thermal stresses caused by the differences in the thermal expansion coefficients of thin films. In addition, the nichrome and copper layers which have been deposited by a thermal evaporation process are highly tensilely stressed (as has been found in other experiments carried out in the past) which may contribute to the failure of the films. Furthermore, there is a potential difference between the plasma and the wafers that contact the grounded cage of the barrel asher. Oxygen ions with plasma electrical potential accelerate due to the presence of the plasma-substrate electric field, bombard the surface of the copper, may enhance the oxidation process and induce additional surface stress.

Failure to integrate the nichrome and copper seed layer with the polyimide sacrificial layer, forced the investigation of a different seed layer. Next, a magnetron sputtered titanium adhesion layer with a nickel seed layer have been investigated.

6.2.1.2 Release of magnetron sputtered titanium adhesion layer and nickel seed layer deposited on top of the polyimide sacrificial layer

Instead of thermally evaporated nichrome adhesion layer/copper seed layer on top of the polyimide sacrificial layer investigated in the previous section, a magnetron sputtered titanium adhesion and nickel seed layers deposited on top of the polyimide sacrificial layer are being investigated in this section.

New wafers with a thermally cured polyimide sacrificial layer and defined anchors have been prepared (fig.6.1a,b). For the deposition of titanium and nickel, a magnetron sputter system is used. Because films which are deposited by magnetron sputtering show excellent sidewall coverage (which is not desirable in lift-off processes), the AZ5214E image reversal photoresist used previously for lift-off of thermally evaporated metallic films would not be suitable for lift-off for use with magnetron sputtered metallic films. A special LOR-5B lift-off resist, which is insensitive to UV radiation and is undercut during the development stage necessary for lift-off, has been supplied by Microchem and has been combined with positive photoresist. The detailed preparation of the lift-off and positive resists, the metal deposition process, lift-off procedure and exposure to etchant for the sacrificial etch are illustrated in figure 6.3.

The recommended spin coating speed for LOR-5B resist is 3000rpm which yields $0.5\mu\text{m}$ thin film. The manufacturer also recommends that the lift-off resist is 1.3 times the thickness of the deposited metal [59]. Therefore, for a 500nm thick nickel metal film a double LOR-5B resist coating is required to provide a clean lift-off process. The first LOR-5B film is coated and baked at 190°C for 60 seconds, followed by coating of an additional LOR-5B thin resist film and a second bake. After deposition and thermal processing of the resists, 50nm titanium followed by $0.5\mu\text{m}$ nickel has been sputtered at 1.5mT work pressure (fig.6.1d). Subsequently the lift-off process has been performed in Megaposit 1165 resist stripper, in ultrasonic bath (fig.6.1e).

In order to concentrate on the release of the metallic seed layer by etching the underlying sacrificial layer, a dry sacrificial etch process has been attempted (fig.6.1h). The dry etch has been

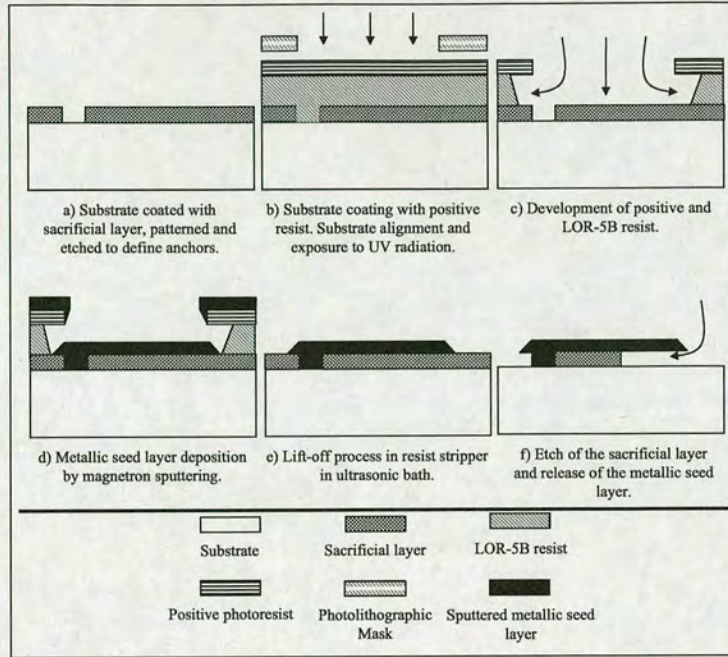


Figure 6.3: Deposition of magnetron sputtered metallic seed layer, pattern by lift-off and release by etch of underlying sacrificial layer.

initially attempted in the barrel asher using trial wafers that have been exposed to O_2 plasma for 120 minutes. After exposure to the plasma, the first observation has been a change of nickel to brown color implying that oxidation has occurred. A scanning electron micrograph of the seed layer after exposure to the plasma is shown in figure 6.4. The adhesion / seed layers have been released only partially and considerable mechanical deformation of the bimetallic thin films is observed in the released areas.

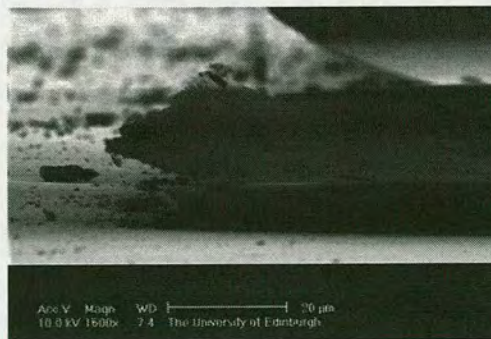


Figure 6.4: Scanning electron micrograph of titanium and nickel layers on top of polyimide sacrificial layer, after 120 minute exposure to O_2 plasma in the barrel asher.

Illustrated in figure 6.5 is a newly available tool that implements a remote O_2 plasma source, and it has also been used for the sacrificial etch of the polyimide thin film and the release of

the adhesion / seed layers. Engineers in the Scottish Microelectronics Center have reported

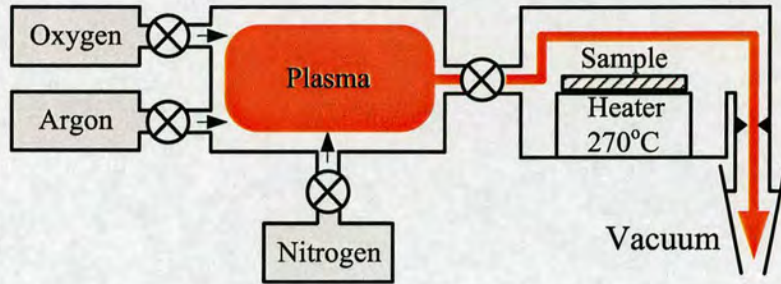


Figure 6.5: Diagram of the remote O_2 plasma source tool.

polyimide undercut rates of up to $12.5\mu\text{m}/\text{min}$ at 10Torr work pressure. However, this undercut rate has been achieved when silicon oxide was used as structural material, without large metal areas on the wafer. Furthermore, the undercut rate in the remote O_2 plasma source tool has been approximately 18 times faster compared to the barrel asher that has been reported to undercut polyimide at approximately $0.69\mu\text{m}/\text{min}$. Here, the wafers have been exposed to O_2 plasma afterglow for 10 minutes. After exposure to plasma afterglow a change in the color of the nickel seed layer has not been observed, implying that the thin films have not been oxidized. Investigation of the etched samples with scanning electron microscopy has shown that the polyimide undercut rate has been approximately only $0.7\mu\text{m}/\text{min}$. This value is ~ 18 times slower than polyimide undercut rates for structures implementing SiO_2 as a structural material. An image of the seed layer after exposure to the O_2 afterglow is shown in figure 6.6.

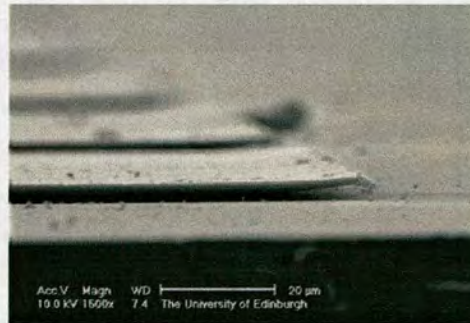


Figure 6.6: Scanning electron micrograph of the nickel seed layer after 10 minute exposure to O_2 afterglow plasma.

The active species of the plasma afterglow is atomic oxygen that can adsorb (adatom) on surfaces, including the chamber sidewalls and the metallic areas on the wafer. Once an atom adsorbs on a surface, another atom that arrives at the surface may recombine with that adatom to form an oxygen molecule, which is not reactive at low temperatures. The probability that

recombination will occur depends on the recombination coefficient (γ) which is 0.27 for nickel, 0.03 for TiO_2 and only 5×10^{-3} - 1×10^{-1} for SiO_2 [60–62], meaning that recombination has a much higher chance of occurring on metallic surfaces. Therefore, the slow polyimide undercut rate observed here is attributed to the high recombination rate of atomic into molecular oxygen on the catalytic nickel and titanium surfaces that cover approximately 95% of the area of the wafer. Essentially these catalytic surfaces cause local recombination of oxygen atoms into molecular oxygen, hence cause local deprivation of atomic oxygen that would have otherwise reached, reacted and etched the underlying polyimide layer.

The metallic seed layer on samples that have been processed in the barrel asher (fig.6.4) appears darker in the SEM compared to the metal which has been processed in the afterglow plasma tool (fig.6.6). This implies that nickel processed in the barrel asher emits less secondary electrons, due to oxidation of the metallic surface. Furthermore, metal processed in the barrel asher (fig.6.4) shows a larger degree of mechanical deformation compared to metal that has been processed in the O_2 plasma afterglow (fig.6.6). These results confirm that ion bombardment effects in the barrel asher (mentioned previously in section 6.2.1.1) affect the stress state of the surface of the metallic film. In-depth discussion of the effects of ion bombardment on solid films can be found in 7.5.

Failure to implement a dry O_2 plasma release of metallic seed layers by etch of a sacrificial polyimide layer using both the barrel asher and the O_2 plasma afterglow, has led to the investigation of a silicon dioxide sacrificial layer for etch in hydrofluoric acid.

6.2.2 Silicon dioxide sacrificial layer for etch in hydrofluoric acid

SiO_2 has been established as a sacrificial layer in MEMS technology, including PDMA processes [63], because of its good process integration and compatibility with other IC materials [64]. SiO_2 is etched in liquid or vapor hydrofluoric acid, which does not react with the nickel seed layer and the Ni-Fe permalloy implemented here.

6.2.2.1 Release of nickel seed layer deposited on top of the SiO_2 sacrificial layer

Initially a $0.5\mu\text{m}$ PECVD SiO_2 sacrificial layer and a $0.5\mu\text{m}$ thin magnetron sputtered nickel seed layer that have been patterned using lift-off were prepared. For the lift-off process positive and LOR-5B resists have been, as illustrated in figure 6.3. After completion of the lift-off

process, samples have been placed in a buffered hydrofluoric acid (BHF) solution, releasing the structures almost immediately (fig.6.1h). However, the released nickel thin film has been very fragile and peeled off the substrate during rinsing and drying of the samples. Electrodeposition of Ni-Fe permalloy on top of seed layer prior to exposure of the samples in wet hydrofluoric acid would strengthen the structures and should increase the fabrication process yield.

This requires the characterisation of the electrodeposition process, which is performed next.

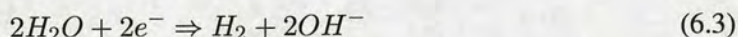
6.3 Characterisation of the electrodeposition process

Electrodeposition of permalloy is performed in electrolytic cell. An electrolytic cell, is composed of the anode, the cathode, an aqueous metal solution containing ions and a power supply. In such a cell, electroplating can take place when an electrical potential appears across the electrodes, initiating electrochemical reactions. The main reactions are:

a) Metal oxidation



b) Hydrogen evolution



c) Metal ion reduction



Oxidation (reaction 6.1) occurs at the anode, resulting in the transfer of metallic ions to the electrolyte solution. At the same time, reduction (reaction 6.4) occurs at the cathode, resulting in the transfer of metallic ions from the electrolyte solution on the surface of the cathode, thus achieving film deposition. Hydrogen is also produced at the cathode through reactions 6.2 and 6.3. Hydrogen formation has metallurgical consequences on the deposited metal and the rate of hydrogen evolution and current density are positively correlated [65]. Figure 6.7 illustrates a simplified electrolytic cell, where a nickel-iron (Ni-Fe) composite is deposited on the cathode. The bath chemistry used for this project has been taken from C. H. Ahn *et al.* [66] and the chemical components are listed in table 6.2. Here a nickel wire (99.0% purity) has been used as the anodic electrode and the electrodeposition process has been characterised initially using a

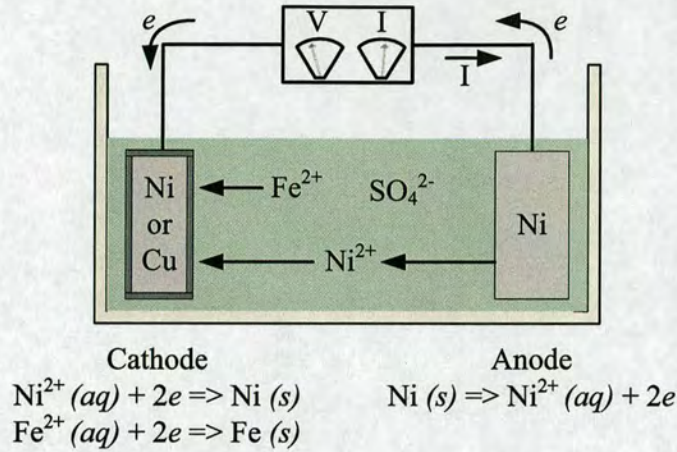


Figure 6.7: A simplified electrochemical cell.

Chemical component	Quantity (g/l)
Nickel Sulfate ($\text{NiSO}_4 \cdot 6\text{H}_2\text{O}$)	200
Boric Acid (H_3BO_3)	25
Ferrous Sulfate ($\text{FeSO}_4 \cdot 7\text{H}_2\text{O}$)	8
Nickel Chloride ($\text{NiCl}_2 \cdot 6\text{H}_2\text{O}$)	5
Saccharin ($\text{C}_7\text{H}_4\text{NO}_3 \cdot \text{S} \cdot \text{Na} \cdot \text{H}_2\text{O}$)	3

Table 6.2: Chemical components of the electroplating bath. Taken from [66].

copper wire as the cathodic electrode. The deposition took place at room temperature and a magnetic stirrer has been used to agitate the solution during the process. Different electrodeposition runs, each run having a different current density, have been performed. The current densities ranged from $60 \mu\text{A}/\text{mm}^2$ to $295 \mu\text{A}/\text{mm}^2$ and the duration of every run has been varied so that the consumed electric charge equalled approximately 7.8 coulombs for each run. Because iron is more readily reducible element than nickel, iron electrodeposits faster than nickel and the solution gets depleted of iron ions in the vicinity of the cathode [67]. A pulsed electrodeposition current (2 second period, 50% duty ratio) has been used here, where the current through the bath is switched off periodically. This allows restoration of the Ni^{+2} - Fe^{+2} ionic equilibrium concentration in the vicinity of the cathode and forms a permalloy with uniform Ni-Fe composition across its thickness.

6.3.1 Morphology of the electrodeposits

After the electrodeposition, the samples have been inspected in the scanning electron microscope and selected micrographs for low and high current densities are shown in figure 6.8. For current densities of $201\mu A/mm^2$ or lower, where hydrogen bubble evolution has not been

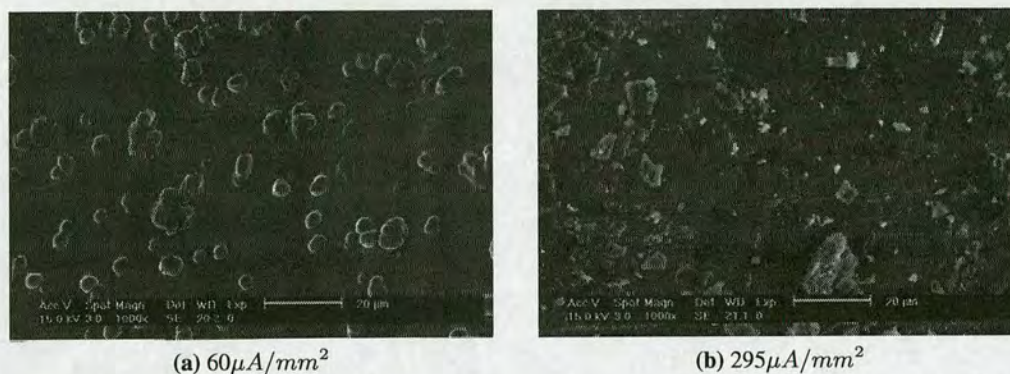
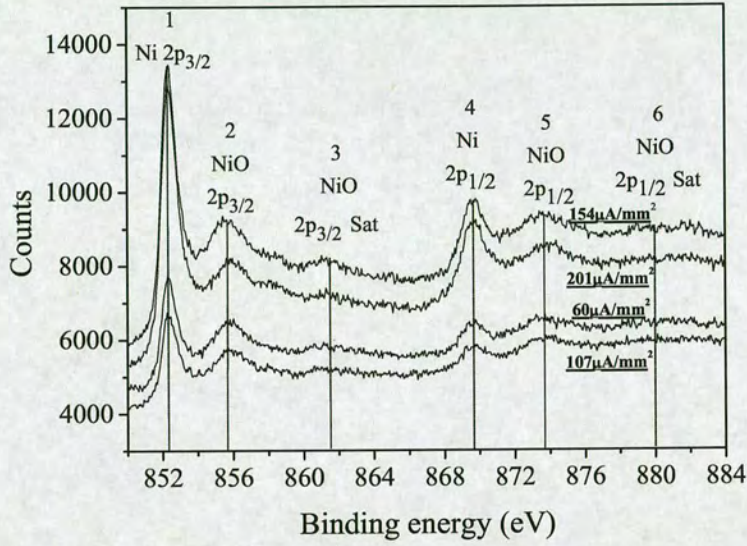


Figure 6.8: *Morphology of the electrodeposited Ni-Fe permalloy and metallurgical effects of H_2 evolution for a) $60\mu A/mm^2$ (no H_2 evolution), and b) $295\mu A/mm^2$ (with H_2 evolution) current densities.*

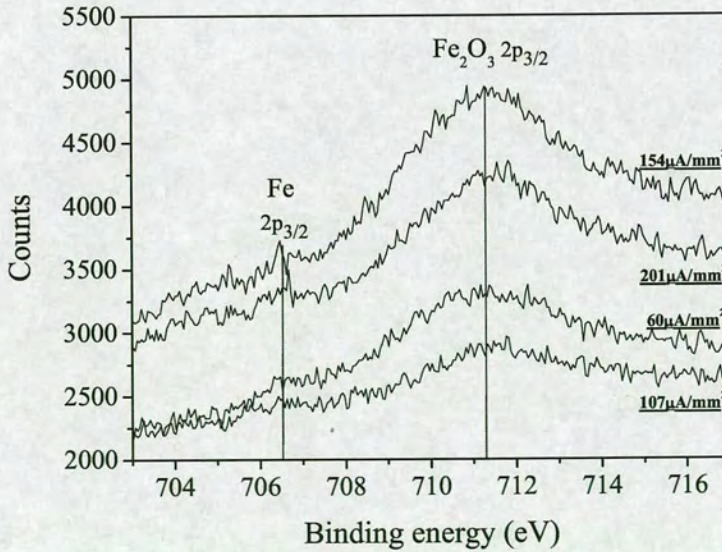
visible during the process, the electrodeposits have smooth granular structure (fig.6.8a), and maintained their color after exposure to the atmosphere. For current densities higher than $201\mu A/mm^2$ where hydrogen bubble evolution has been visible, the surface of electrodeposited material appeared less smooth (fig.6.8b), and after short exposure to the atmosphere a color change has been observed implying oxidation of the deposited metal. To confirm that the electroformed film contains both nickel and iron, chemical analysis has been performed next.

6.3.2 Chemical composition of the electrodeposits

Energy dispersive X-ray spectroscopy would have been the ideal analytical method for the characterisation of the chemical composition of the electrodeposits due to the rapid analysis of large areas and because its high sampling depth minimizes errors originating from surface contamination and oxidation. However, energy dispersive X-ray spectroscopy has not been available and X-ray photoelectron spectroscopy (XPS) has been employed. The main disadvantage of XPS is the very shallow sampling depth, which renders the analysis results sensitive to surface contamination and oxidation. New samples have been prepared by exactly the same electrodeposition conditions described in the beginning of section 6.3 with pulsed current densities less



(a) Nickel 2p XPS spectra



(b) Iron 2p XPS spectra

Figure 6.9: X-ray photoelectron spectra for a) nickel and b) iron. The electrodeposition current density is indicated for each curve.

than $201\mu A/mm^2$ (H_2 bubble evolution has not been observed to occur for current densities less than $201\mu A/mm^2$). The samples have been loaded into the XPS equipment immediately after the completion of the electrodeposition process. After loading the samples in the instrument, the chamber has been pumped down to 10^{-9} Torr pressure. Next, the sample surfaces have been cleaned for 360 seconds using an argon milling ion beam in order to remove as much contamination as possible. Subsequently, a monochromatic Al $K\alpha$ ($h\nu = 1486.6\text{eV}$) X-ray source operating at 15kV at 30 degrees incident angle has been used for the analysis. The instrument employed an electron source that replenished the sample's emitted electrons, thus eliminating the charging effect.

The resulting Ni 2p X-ray photoelectron spectra are illustrated in figure 6.9a. Peak number 1 at 852.4eV and the peak number 4 at 869.6eV are associated with metallic nickel, $2p_{3/2}$ [68] and $2p_{1/2}$ [69] shells respectively. Peak 2 at 856eV and its satellite peak number 3 at 860.6eV correspond to NiO $2p_{3/2}$ shell [68]. Peak 5 at approximately 873.5eV corresponds to NiO, shell $2p_{1/2}$ and peak 6 at 880eV is the satellite peak [69].

For the iron XPS spectra, illustrated in 6.9b, 2 main peaks are present. It can be seen in figure 6.9b that the $2p_{3/2}$ peak corresponding to oxidized iron (Fe_2O_3) at 711.3eV dominates the metallic Fe $2p_{3/2}$ peak at 706.6eV. The strong presence of iron oxide may be due to oxidation of the film surface after exposure to the atmosphere.

XPS analysis has shown that the electrodeposit contains both iron and nickel at current densities less than $201\mu A/mm^2$ where hydrogen bubble evolution has not been observed to occur. After chemical characterisation of electroformed permalloy, the plating uniformity on wafer scale is investigated next.

6.3.3 Wafer scale electrodeposition and thickness uniformity

For the investigation of the plating uniformity on wafer scale, new wafers have been prepared with a SiO_2 sacrificial layer, with defined anchors and a $0.5\mu\text{m}$ magnetron sputtered nickel seed layer (fig.6.1a-e). Subsequently a $15\mu\text{m}$ thick SPR220.7 mold has been patterned on the substrate to define the electrodeposition areas (fig.6.1f). The design layout of patterned photoresist mold can be seen in figure 6.10, where during electrodeposition the bright areas are filled with Ni-Fe. After the photoresist mold has been patterned, its profile has been obtained

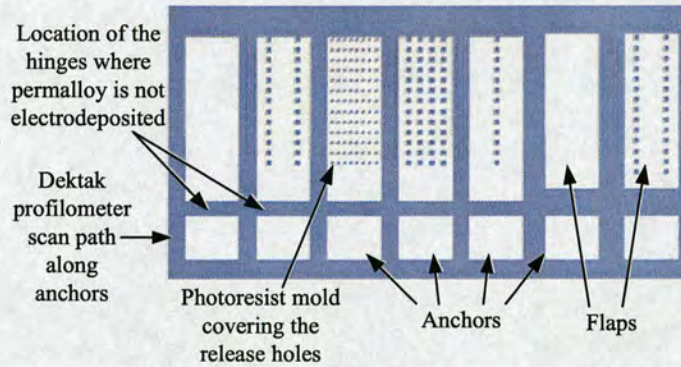


Figure 6.10: Top view of an array of structures. The bright areas indicate exposed nickel seed layer where permalloy is electrodeposited. Gray areas represent the photoresist mold where electrodeposition is inhibited.

by dektak profilometry along the location of the anchors, as can be seen in figure 6.11a. Next the electroforming process has been performed (fig.6.1g). The current was 30mA, pulsed with 2 second period and 50% duty ratio, and the electrodeposition duration was 120 minutes. After the electrodeposition, the wafer has been profiled in various locations (scan path along the anchors is indicated in figure 6.10) and selected profiles obtained with dektak are shown in figures 6.11b,c.

In figure 6.11b it can be seen that the trenches defined by thick photoresist mold have been partly filled with nickel-iron. Comparison of the trench depths from profilometry scans before (fig.6.11a) and after the electrodeposition (fig.6.11b) indicates that the thickness of electrodeposited Ni-Fe is approximately $15\mu\text{m} - 11.4\mu\text{m} = 3.6\mu\text{m}$, yielding deposition rate of 30nm per minute. The thickness of the electrodeposited permalloy of this scanned sample has been uniform.

However, the same uniformity is not always observed across the wafer. Profiles of trenches where the surface of the electrodeposit has been rougher can be seen in figure 6.11c. Fur-

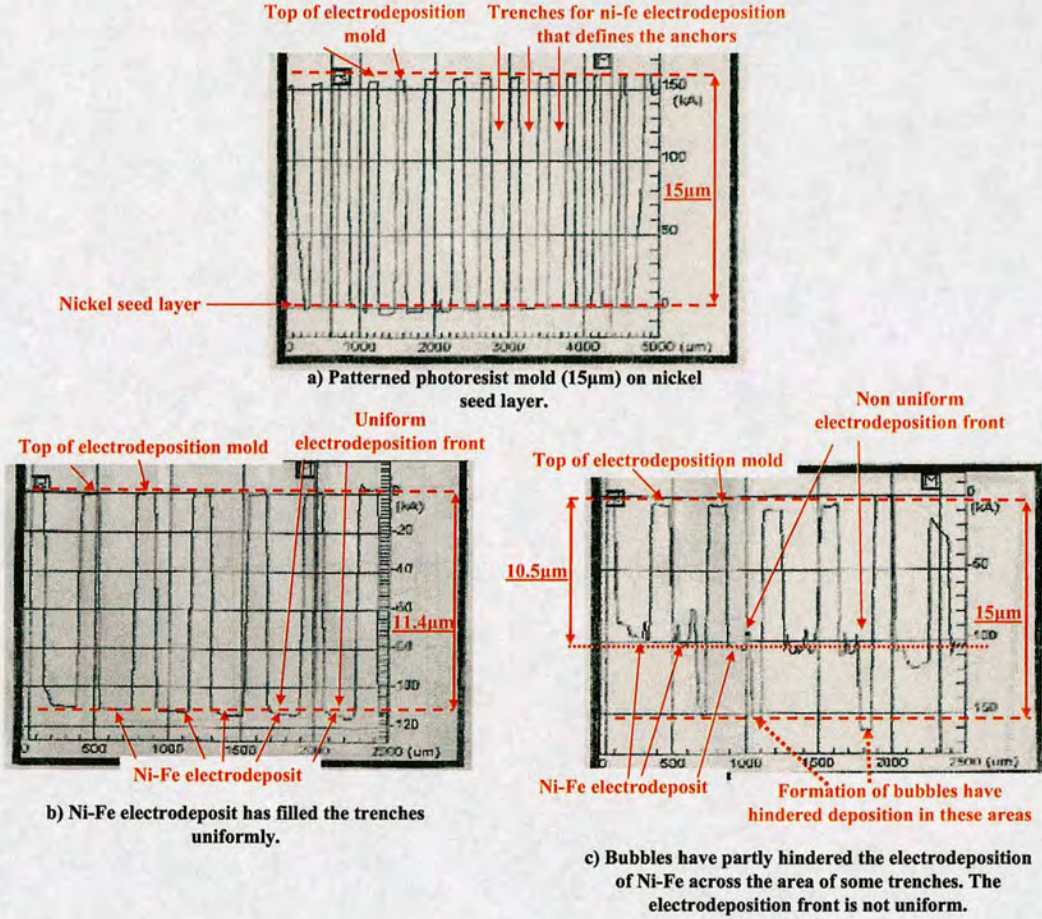


Figure 6.11: Profiles of a) patterned thick photoresist mold, b) uniformly electroformed Ni-Fe, and c) non-uniformly electroformed Ni-Fe due to formation of H_2 bubbles.

thermore, in some positions inside the trenches illustrated in figure 6.11c, permalloy has not been electrodeposited. This is most likely due to the formation of H_2 bubbles by the evolution reactions (equations 6.2 and 6.3) on the surface of the nickel seed layer. Formation of H_2 bubbles on the seed layer have been known to hinder further permalloy electrodeposition [70]. Further inspection of the wafer has shown that this effect appears in random locations across the substrate. Because the structures have not been released yet, it is not known whether this side-effect compromises the functionality of the structures.

After deposition of a $\sim 3.6\mu m$ thin permalloy, the $15\mu m$ thick SPR220.7 photoresist mold has been removed in acetone followed by bath in isopropanol. The release process of the structures by etch of the sacrificial SiO_2 in hydrofluoric acid and the magnetic assembly is investigated

next.

6.4 Demonstration of plastic deformation magnetic assembly

In section 6.2.2 the nickel seed layer has been successfully released by sacrificial etch of an underlying PECVD SiO₂ layer in hydrofluoric acid. To full develop the PDMA process, nickel-iron has to be electrodeposited on a metallic nickel seed layer prior to releasing the structures. The electrodeposition process has been characterised in the previous section where samples have been fabricated and include: i) a PECVD SiO₂ sacrificial layer, ii) a nickel seed layer, and iii) an electroformed Ni-Fe permalloy on top of the nickel seed layer. In the next sections the composite nickel seed layer – Ni-Fe permalloy is released by sacrificial etch of the PECVD SiO₂ layer in wet and vapor hydrofluoric acid.

6.4.1 Release in wet buffered hydrofluoric acid solution

To release the nickel–Ni-Fe flaps, the sample has been placed in buffered hydrofluoric acid solution and the release of the structures has been almost immediate (fig.6.1h). Due to their fragility, many flaps have been ripped off the substrate during the rinsing and drying process that follows the hydrofluoric acid etch.

Following the release of the flaps, the substrate has been exposed to the permanent field of a magnet supplied with the Balzers magnetron sputter system (fig.6.1i). As the substrate has been moved above the magnet, the remaining released structures deformed at the location of the hinge (fig.6.1j), aligned to the magnetic field and oriented perpendicularly to the substrate. When the substrate has been moved away from the permanent magnet the flaps intersected with the flux lines causing in many cases their deformation back to their initial horizontal state on the surface of the substrate. After this process the substrate has been inspected in the scanning electron microscope and micrographs of selected samples can be seen in figure 6.12. Areas where deposition of Ni-Fe permalloy has been inhibited due to the formation of H₂ bubbles (discussed earlier in section 6.3.3) are indicated. As can be seen in the micrograph, many flaps have been ripped off the substrate during the post release rinsing and drying process, resulting in low yield fabrication process. One way to improve the yield of the process is to heat the hydrofluoric acid solution and expose the substrate to the fumes, thus avoiding the wet bath, rinsing and drying of the samples. Fukuta *et al.* have invented a novel HF vapor release method

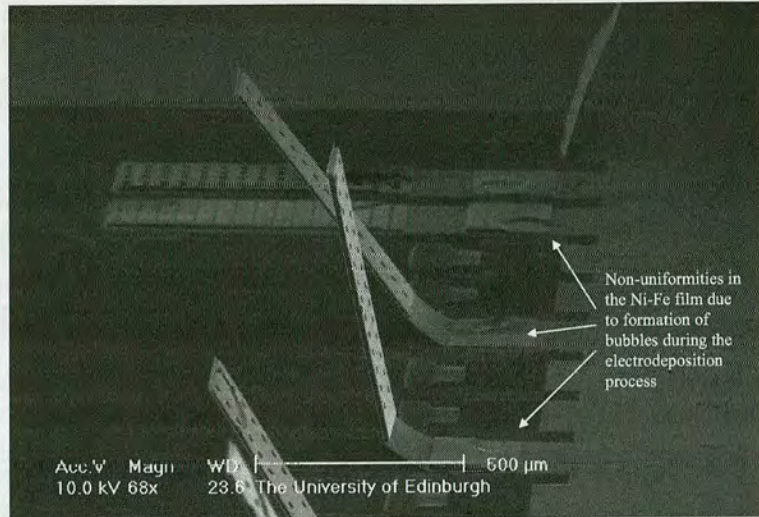


Figure 6.12: A scanning electron image of plastically deformed and magnetically assembled out of plane flaps. Non-uniformities in the Ni-Fe thickness due to the formation of H_2 bubbles are indicated. The wet HF release method is a low yield process.

where a bulb is used to heat a small quantity of hydrofluoric acid solution, causing HF fumes that etched the SiO_2 [71]. Memstar (a research and development company in the Scottish Microelectronics Centre) has been developing a tool that uses hydrofluoric acid vapor for etch of SiO_2 thin films and is ideal for the release of the structures here because post-release sample rinsing and drying would not be required. Next the release of nickel–Ni-Fe permalloy flaps in vapor hydrofluoric acid is described.

6.4.2 Release in vapor hydrofluoric acid

The Memstar tool is advantageous because it achieves dry etch of the sacrificial SiO_2 layer and release of composite nickel seed layer – Ni-Fe permalloy structures. The dry release approach does not require post-release rinsing and drying of samples, which has previously shown to reduce the fabrication process yield, hence an increase in the yield is anticipated when the tool from Memstar is implemented for our release process.

The diagram of the Memstar tool used for the release of the structures here is illustrated in figure 6.13. During the etch phase, HF vapor is injected into the chamber and may combined with H_2O vapor, which has catalytic function and accelerates the etch process [71]. After the etch step, the chamber is purged with N_2 . Due to the commercial sensitivity, the etch conditions have not been made known. Samples have been processed in the tool and after a 10 minute trail

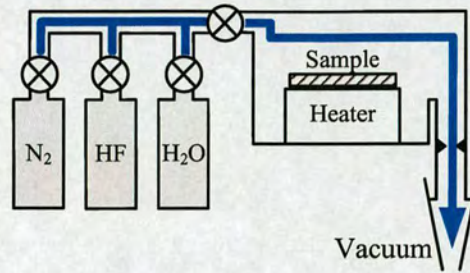
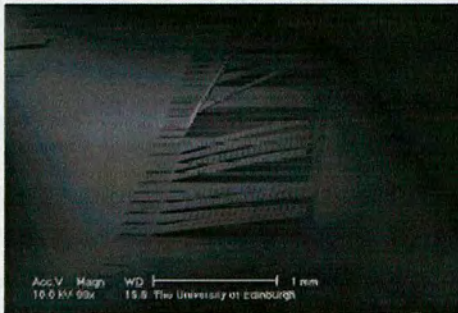


Figure 6.13: Schematic of Memsstar's vapor hydrofluoric acid etch tool.

etch process most of the structures were released. Following the successful release of the flaps, the magnetic deformation assembly process has been performed using a magnet.

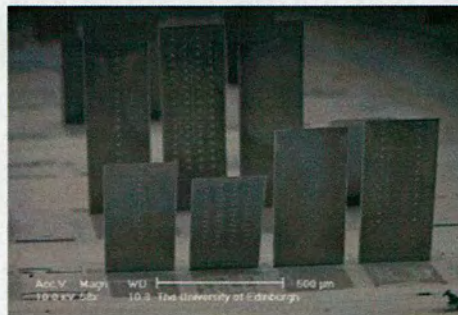
The samples have been carefully inspected in the SEM and it has been established that the yield of the hydrofluoric acid vapor release process is 100%. Scanning electron micrographs of released and deformed flaps can be seen in figure 6.14.



(a) Perspective of released flaps.



(b) Front view of magnetically deformed out of plane flaps.



(c) High magnification of (b).

Figure 6.14: Scanning electron images of plastically deformed and magnetically assembled out of plane flaps through the use of a high yield HF vapor release process.

As the substrate has been moved above the magnet, the remaining released structures deformed at the location of the hinge (indicated in figure 6.1i), aligned to the magnetic field (fig.6.1j) and oriented perpendicularly to the substrate. As the substrate has been moved away from the permanent magnet the flaps intersected with the flux lines causing majority of the flaps to deform back to their initial horizontal state on the surface of the substrate. One way of producing permanently deformed structures is to place the substrate in a beaker which rests on the magnet. Under the influence of the magnetic field, the structures will deform out of plane and an electro-less solution can be added in the beaker to form an additional nickel layer on the structures. The hinges would be reinforced to provide the necessary rigidity to maintain the flaps deformed out of plane, at all times.

6.5 Conclusion

Thermally cured polyimide sacrificial thin film for etch in O₂ plasma aiming to release overlying metallic layers (nichrome adhesion layer/copper seed layer and titanium adhesion layer/nickel seed layer) has been investigated in section 6.2.1. The release of structures in O₂ plasma, in the barrel asher, has been unsuccessful due to oxygen ion bombardment that ruined the seed layers. Furthermore, polyimide etch in the barrel asher as well as in atomic oxygen plasma afterglow has been unsuccessful due to the recombination of reactive atomic oxygen into molecular non-reactive oxygen on the catalytic metallic surfaces of the adhesion and seed layers. Since the use of polyimide as sacrificial layer for release of metallic seed layer in O₂ plasma has not been successful, alternative sacrificial layer/release methods have been investigated.

The implementation of a PECVD SiO₂ sacrificial layer for etch in hydrofluoric acid and the release of overlying nickel seed layer has been successful in section 6.2.2.

Subsequently the morphology (section 6.3.1), chemical composition by X-ray photoelectron spectroscopy (section 6.3.2) and wafer electrodeposition uniformity (section 6.3.3) have been characterised. For electrodeposition on wafer scale, the Ni-Fe permalloy electrodeposit thickness has been found to not be always uniform. This is believed to be due to the formation of H₂ bubbles on the surface of the nickel seed layer, that inhibit the deposition of additional Ni-Fe permalloy after H₂ bubbles have formed.

Finally the plastic deformation magnetic assembly process has been demonstrated in section 6.4, where wet and vapor hydrofluoric acid has been used to etch the PECVD SiO₂ layer and

subsequently release the overlying composite nickel seed layer – Ni-Fe permalloy structures. Although the wet release has been a low yield process, sacrificial etch of SiO₂ in Memsstar's hydrofluoric acid vapor tool has been a fabrication process with 100% yield. Plastic deformation magnetic assembly of the released structures by their exposure to a magnetic field has been demonstrated. Further work would include strengthening the flaps at the location of the hinges by additional electro-less deposition of nickel, on top of the deformed structures. For the convenience of the reader, the complete fabrication process flow can be found in appendix C.

Chapter 7

Relaxation of process-induced surface stress in amorphous silicon carbide thin films using low energy ion bombardment

As mentioned in the introduction of this thesis, due to its excellent semiconducting and mechanical properties, thermally grown silicon carbide is a promising material for MEM devices. In section 7.1 is made a brief introduction to the electro-mechanical properties of SiC and the available deposition methods. In this chapter cantilever beams of PECVD amorphous silicon carbide thin films are fabricated with various processes. It has been found that the fabrication process can induce a surface stress in the α -SiC thin film causing out of plane deflection of structures. The fabrication induced stress could be relaxed when the surface of the thin film has been bombarded with low energy argon ions, causing the elimination of the deflection of the microstructures. White light interferometry has been used to monitor the mechanical deformation of the cantilever beams, to characterise the stress induction and the stress relaxation process. The next section provides a brief introduction to the properties of silicon carbide and the available deposition techniques.

7.1 Silicon carbide material properties and deposition techniques

3C-, 4H- and 6H- are three crystalline silicon carbide polytypes that find wide application in the microelectronics industry. The polytypes are distinguished by differences in the stacking sequence of silicon and carbon planes resulting in differentiation of the electrical properties of the three polytypes. For example, the bandgap is 2.3eV in 3C-SiC, 2.99eV in 6H-SiC and 3.4eV in 4H-SiC. Additional differences exist in the hole and electron mobilities and electron saturated drift velocity in the polytypes. The SiC polytypes also exhibit different mechanical properties. The linear thermal coefficient of expansion [$10^{-6}/K$] is 2.9 in 3C-SiC and 4.2 in

6H-SiC [72]. The elastic modulus of 3C-SiC is approximately 370GPa [73] and can be as high as 794GPa for aluminium doped films [72]. The modulus for 6H-SiC is reported to range between 392GPa and 470GPa [74].

Silicon carbide is commonly deposited by the decomposition of gas precursors containing silicon and carbon in a high temperature, atmospheric pressure or low pressure chemical vapor deposition reactor. Silicon and carbon atoms recombine on a suitable susceptor, which is heated to the desired temperature by radio frequency induction, to form SiC. One key parameter is the deposition temperature that determines the resulting SiC polytype. Single crystalline 3C-SiC can be synthesized at roughly 1300°C. This temperature is lower than the melting point of silicon (1410°C) and enables the growth of crystalline 3C-SiC directly on silicon substrates. However, 6H-SiC is grown at roughly 1700°C and is not compatible with silicon substrates, but requires a graphite coated SiC susceptor. Polycrystalline 3C-SiC is more versatile because it can be grown on various surfaces including SiO₂, polycrystalline silicon and Si₃N₄ at deposition temperatures ranging from 1050°C to 1250°C. Amorphous SiC (*a*-SiC) can be deposited on a wide range of substrates by low temperature (200°C-400°C) plasma enhanced chemical vapor deposition method. Amorphous SiC can be recrystallized after the deposition by a high temperature anneal process [72]. The low cost of PECVD renders *a*-SiC an attractive material for application in MEMS. In this chapter the suitability of PECVD *a*-SiC films deposited on silicon substrates for application in MEMS is investigated.

7.2 The effect of stress in the mechanical deformation of microstructures

A stressed thin film will tend to expand or contract depending on whether it is in a compressive or tensile state. Before the release of the microstructures, traction between the thin film and the substrate does not allow the relief of the stress. Once the structures have been released, the stress in the film that defines the microstructures is relieved causing mechanical deformation [of the structures]. A released bridge fabricated of a material with compressive stress would tend to buckle, while a cantilever beam would experience an elongation towards the free end and a small out of plane deflection towards the substrate, due to a rotation that originates in the boundary of the microstructure [75]. Another type of stress that causes mechanical deformation of released microstructures is a stress gradient across the thickness of the thin film that defines

the microstructures. In a released cantilever beam, the relief of a stress gradient effectively causes a moment M to appear across the length of the cantilever. This results in constant curvature and a non-linear deflection δ_f of the unrestrained end of the cantilever, defined by equation 7.1.

$$\delta_f = \frac{M \times L^2}{2 \times E \times I} \quad (7.1)$$

where M is the moment, L is the length of the cantilever, E is the modulus of elasticity and I is the second moment of the cross-sectional area of the cantilever beam.

7.2.1 Calculation of the curvature

Calculating the curvature of a deformed structure can assist in determining the nature of the stress that causes the deformation. In order to calculate the curvature, the deflection profile of the structures has to be reconstructed accurately using collected data points from interferometric measurements.

The reconstruction of the deflection profile (AB) of a cantilever beam from interferometric data points (a,b,c, ... g) is illustrated in figure 7.1, where the non-linear path AB is approximated with linear paths ab, bc, cd, ... fg.

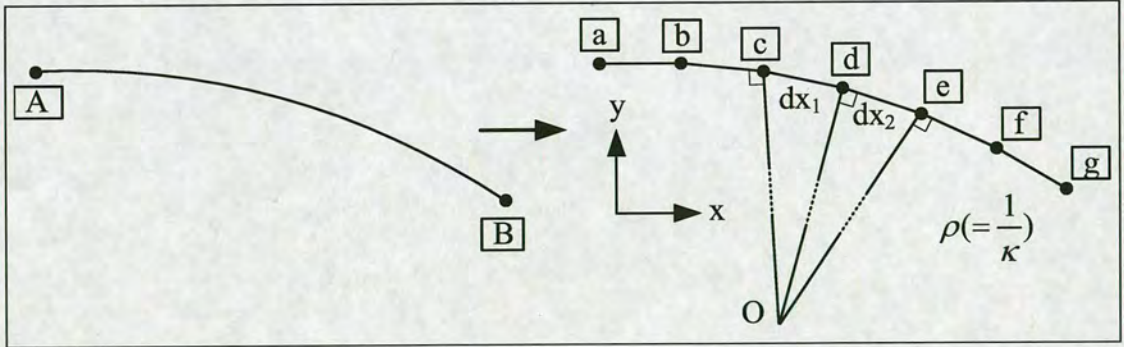


Figure 7.1: Transformation of a non-linear path into a sum of small linear parts. The radius of curvature is denoted by the Greek letter ρ .

The profile AB is approximately equal to

$$AB \simeq \sum ab, bc, cd, de, ef, fg \quad (7.2)$$

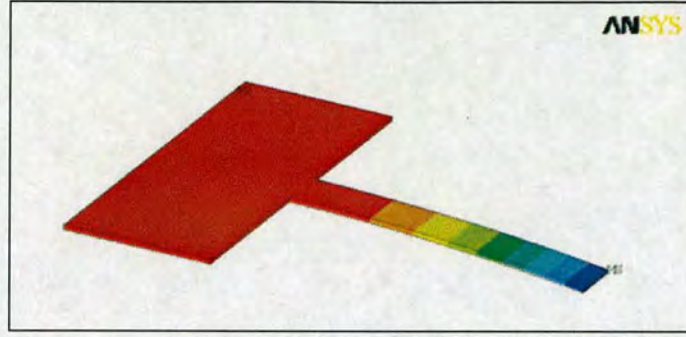
Obviously, the accuracy of equation 7.2 increases as the number of terms on the right hand side increase. With reference to figure 7.1, the curvature $k(= \frac{1}{\rho})$ is calculated using the formula:

$$k = \frac{\tan^{-1} \frac{dx_e - dx_d}{dy_e - dy_d} - \tan^{-1} \frac{dx_d - dx_c}{dy_d - dy_c}}{\sqrt{(dx_e - dx_c)^2 + (dy_e - dy_c)^2}} \quad (7.3)$$

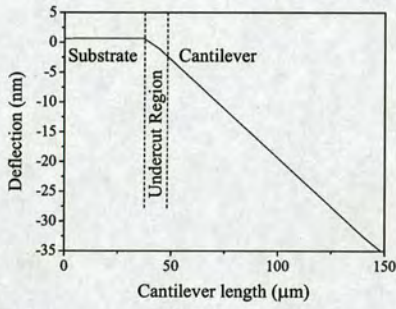
where x_a is the coordinate of point a on the x axis, y_a is the coordinate of point a on the y axis, etc.

7.2.2 ANSYS Finite element modeling of stressed cantilever beams

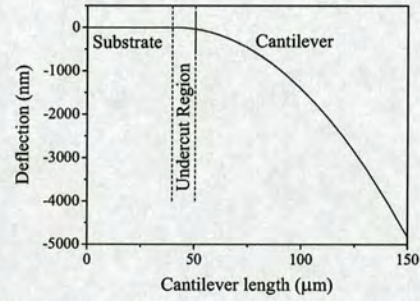
To investigate the contribution of a mean stress and a stress gradient in the deflection of cantilever beams, ANSYS finite element modeling simulations have been performed. To reproduce accurately the boundary conditions of the microstructures, including the undercut of the silicon substrate, a 3-dimensional model using SOLID95 tetrahedral elements has been programmed. The finite element model is displayed in figure 7.2a. For the simulations, 370GPa Young's modulus and 0.16 Poisson's ratio has been assumed [73], although the material properties of the a-SiC used here may be different from these values. The cantilever length has been $100\mu\text{m}$, the width has been $15\mu\text{m}$ and the thickness has been $1.5\mu\text{m}$. Figures 7.2b and 7.2c illustrate the simulated deflection profiles of the a-SiC cantilever beams under the effect of a mean stress (160MPa) and a stress gradient (390MPa/ μm) respectively. It can be seen that the maximum deflection that occurs at the tip of the cantilever beam due to the mean stress (fig.7.2a) accounts for 1.5% of the deflection due to a stress gradient (fig.7.2b).



(a) Finite element model of deflected cantilever beam due to a mean stress and a stress gradient.



(b) Deflection profile due only to the mean stress of 160 MPa.



(c) Deflection profile due only to the stress gradient of 320 MPa/μm.

Figure 7.2: Deflection profiles of released, pre-stressed cantilever beams obtained by ANSYS simulations. The simulated undercut is 8 μm deep.

7.3 Fabrication of α -SiC microstructures

In this section microstructures made of amorphous SiC are defined using reactive ion etch. The PECVD amorphous SiC film used here has been deposited on 3-inch wafers by Oxford Plasma Technology at 400°C. The film has been 1.5 μm thick and the mean residual stress of the film has been measured to be compressive at 160 MPa. To further process the material, the wafer has been diced in 1 cm² pieces. A 2 μm thick, compressively stressed, high frequency PECVD SiO₂ film has been deposited on the samples to act as a hard mask during the etch of the SiC film (process 'A')(fig. 7.3a). Next, the samples have been photolithographically patterned and the SiO₂ layer has been etched anisotropically in a CF₄/H₂ plasma, exposing the underlying SiC layer (fig. 7.3b). Next, the SiC layer has been etched anisotropically in a SF₆/O₂ inductively coupled plasma using the optimized etch conditions reported by L. Jiang *et al.* [76] (fig. 7.3c). More specifically, the gas flows have been 40 sccm and 10 sccm for SF₆ and O₂ respectively,

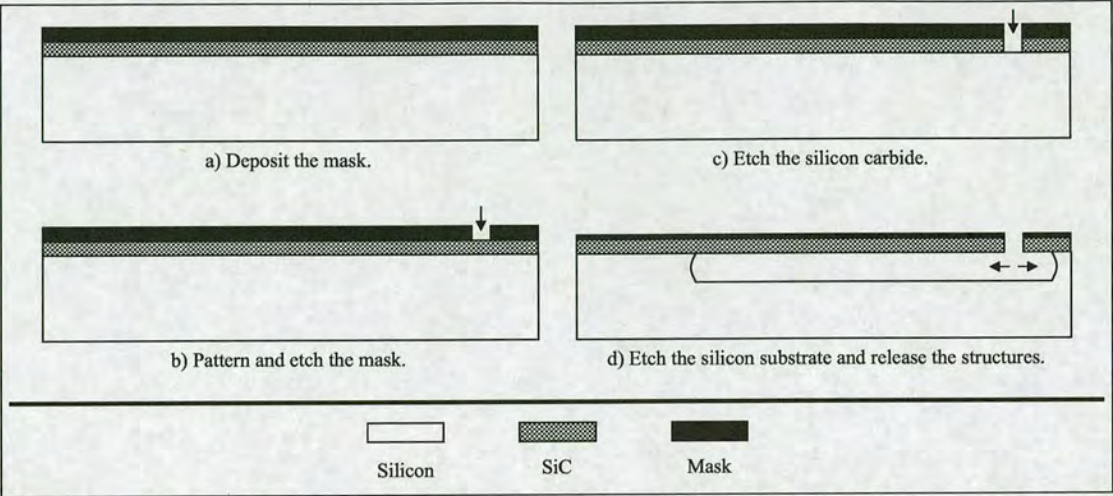


Figure 7.3: *Fabrication process for the SiC microstructures.*

the work pressure has been 5mT, the coil power has been 1000W and the bias power has been 50W. In these conditions, the SiO₂ etch rate has been 134nm/min and the SiO₂/SiC selectivity has been slightly less than 1. After the etch of the SiC film, the SF₆/O₂ etch continued and the silicon substrate has been removed isotropically, releasing the microstructures (fig. 7.3d). The remaining SiO₂ has been subsequently removed in a CF₄/H₂ plasma. The resulting microstructures included cantilever beams and bridges with 25, 50, 100 and 150μm lengths, 15μm width and 1.5μm thickness. The samples have been inspected in the SEM and the cantilever beams and bridges, shown in figure 7.4, have been found to deflect severely.

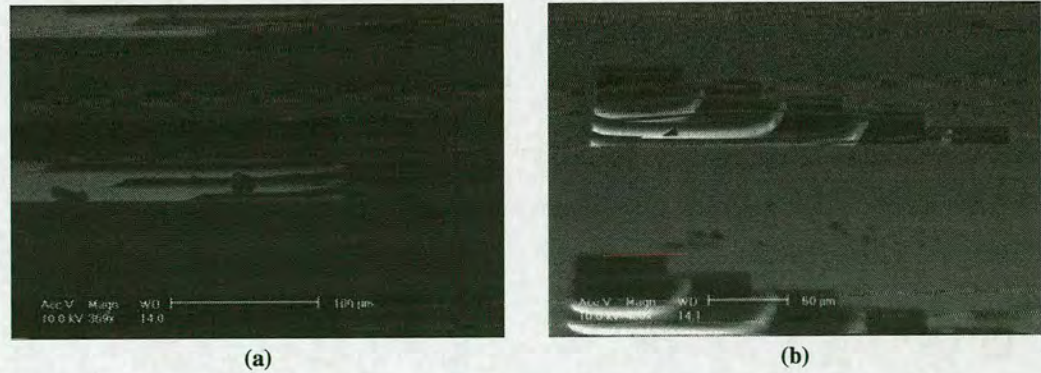


Figure 7.4: *SEM images of fabricated silicon carbide microstructures.*

The fabrication process has been modified by altering the masking material and eliminating the dry etch step that served to remove the mask. a-SiC cantilevers have been fabricated using a 0.5μm thick, mixed frequency low stress (process ‘B’), as well as highly tensile (process ‘C’)

PECVD SiN, deposited at 300°C. Because of the low selectivity between the SiN and a-SiC (4:1) in the SF₆/O₂ plasma, an additional 1.35µm thick SiO₂ film has been deposited, thus forming a sufficiently thick SiO₂/SiN mask on the a-SiC. After the pattern and etch of the hard mask, the etch of the SiC layer and the subsequent release of the structures, the SiO₂/SiN mask has been removed in a buffered HF solution. The fourth etch mask investigated has been 100nm thin nichrome, thermally evaporated onto the a-SiC surface at 1.5×10^{-2} mT work pressure. The nichrome mask has been photolithographically patterned and selectively removed by wet etchant (TFC nichrome etchant), exposing the SiC. After the SiC cantilevers etch and release in SF₆/O₂ plasma, the remaining NiCr mask has been removed by a wet etch step (process 'D'). Table 7.1 summarizes the different type of masking materials and the mask removal methods used in the fabrication processes.

Process	Masking material	Mask removal
A	PECVD SiO ₂ (compressive)	Dry etch (CF ₄ /H ₂)
B	PECVD SiN (low stress) + PECVD SiO ₂	Wet etch (buffered HF)
C	PECVD SiN (tensile) + PECVD SiO ₂	Wet etch (buffered HF)
D	Thermally evaporated nichrome (tensile)	Wet etch (TFC Nichrome etchant)

Table 7.1: *Summary of the fabrication processes.*

Compared to microstructures fabricated with process 'A', the cantilevers fabricated with processes 'B', 'C' and 'D' have relatively small deflection profiles, implying the absence of a stress gradient in the a-SiC after release. This observation suggests that the deposition of a PECVD SiO₂ film and/or the exposure to ion bombardment (during the mask removal stage) in fabrication process 'A' could have caused changes in the stress state of surface of the a-SiC.

The deflection profiles of samples fabricated with process 'A', 'B' and 'C' have been measured using white light interferometry and are plotted in figure 7.5. Next the microstructures fabricated with process 'A' have been bombarded with ionic argon in ICP reactor and the effects in the deflection of the cantilever beams are presented next.

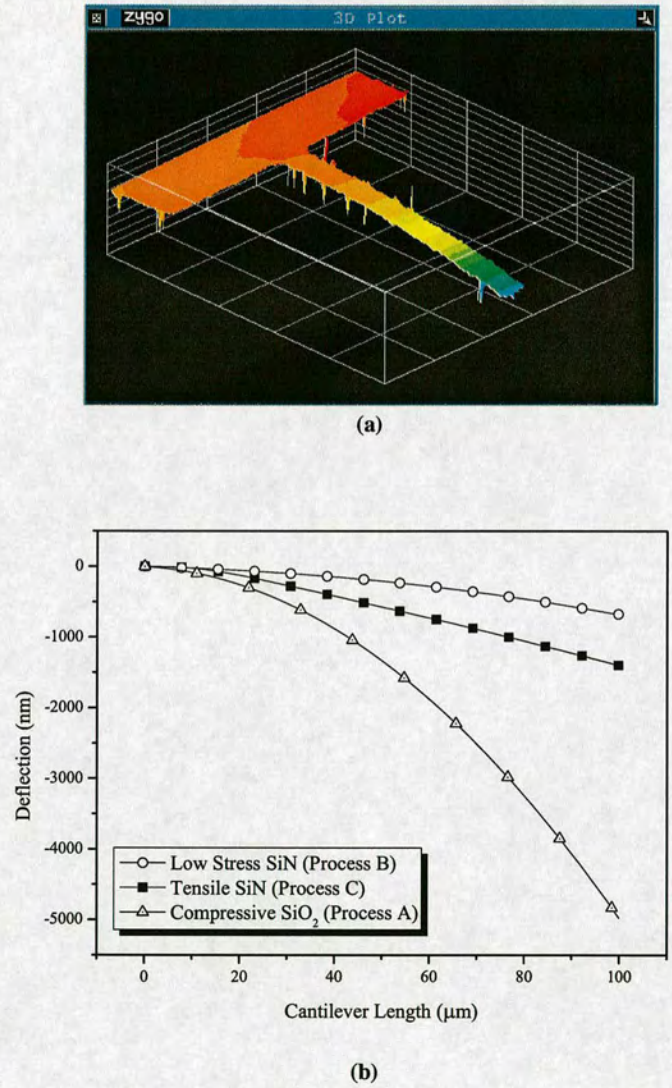


Figure 7.5: A 3-D Zygo plot of a) a 100µm long cantilever beam fabricated with process 'A' and b) profiles of 100µm long beams fabricated with processes 'A', 'B' and 'C', after the removal of the mask.

7.4 The effects of argon bombardment in the a-SiC thin film

Samples that have been fabricated using process 'A' showed the largest mechanical deformation and have been bombarded with low energy argon ions using an ICP reactor. This experimental setup offers several advantages. First, argon is an inert element and no chemical reaction with the target a-SiC material would occur. Secondly, the ICP reactor allows, among other parameters, the separate control of the ion flux by adjustment of the coil power and the energies of the incident ions by adjustment of the substrate power [77]. Here, only the substrate bias has been varied while maintaining all other processing parameters constant. More specifically, the coil power has been 500W, the argon gas flow has been 40sccm, the work pressure has been 10mT and the platen power has been varied to produce a DC bias ranging from 100V to 250V at 13.56MHz frequency. Initially a sample has been exposed to argon plasma for 60 seconds, 120 seconds and 180 seconds at 100V DC bias and the deflection profiles of cantilever beams have been obtained using white light interferometry after each exposure. Figure 7.6 illustrates the recovery of the deflection profile of a selected 100 μ m long cantilever beam before and after each exposure to plasma. Additional samples fabricated with process 'A' have been bombarded with ionic argon at higher energies (100-250eV) and the results are discussed in the next sections.

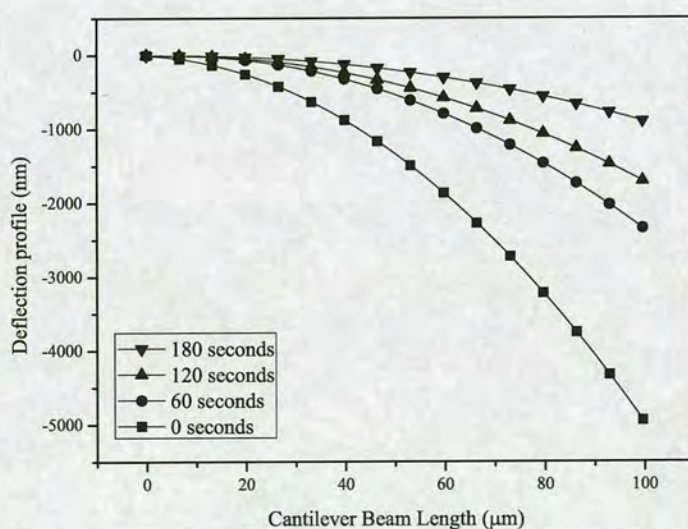


Figure 7.6: Deflection profiles of a selected 100 μ m long cantilever beam, before and after exposure to the plasma for 60, 120 and 180 seconds at 100V bias voltage. The cantilever beam has been fabricated using process 'A'.

7.4.1 Curvature calculations of the cantilever beams

In this section samples fabricated with process ‘A’ have been bombarded with ionic argon at 100eV, 150eV and 200eV energies in ICP reactor for 60, 120 and 180 seconds and the interferometric results have been used to calculate the curvature of the microstructures before and after each exposure to plasma according to the method described in subsection 7.2.1. 255 data points have been collected during the interferometric measurements, regardless of the cantilever lengths, meaning that the distance between two consecutive data points has been $0.58\mu\text{m}$ for the longest ($150\mu\text{m}$) cantilever and only 125nm for the shortest ($25\mu\text{m}$) cantilevers.

The curvatures of the deflected cantilever beams have been calculated using formula 7.1, have been averaged across all samples and have been plotted in figure 7.7 against exposure time to argon ion bombardment. The calculated average curvature has been found to be constant along the lengths of the cantilevers, implying the presence of a constant moment due to the stress gradient in the *a*-SiC film. The finite element modeling simulation results from section 7.2.2, the interferometric deflection profiles (fig.7.6) and curvature calculations (fig.7.7) suggest that the observed non-linear deflection profile introduced by the presence of a stress gradient, being proportional to the square of the length, is the dominant factor that determines the mechanical deformation of the microstructures here.

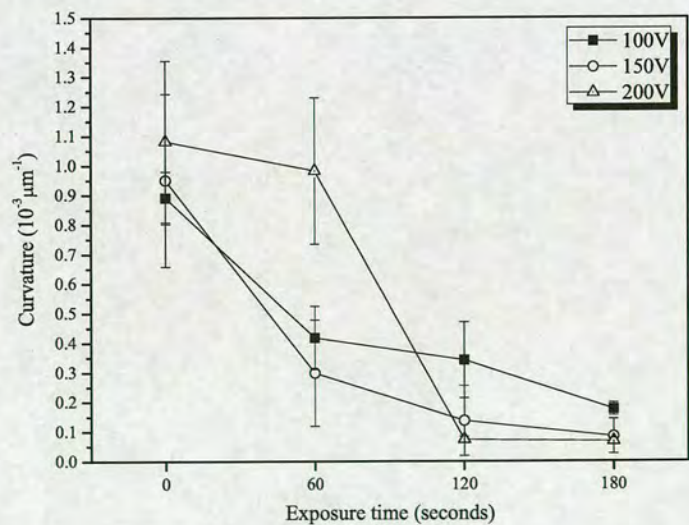


Figure 7.7: Plot of the average curvature of the samples for various ion bombardment energies. The vertical error bars indicate the average standard deviation of the samples.

7.4.2 The effect of exposure duration in the recovery of the deflection

In this section samples fabricated with process ‘A’ have been bombarded with ionic argon at 100eV, 150eV, 200eV and 250eV energies in ICP reactor for 60, 120 and 180 seconds and the interferometric results have been used to determine the change in the deflection of the tip of the microstructures before and after each exposure to the plasma.

The deflection of the tip of the cantilever beams obtained from the interferometric measurements have been plotted for all microstructure lengths and plasma treatment conditions (time and ion energy), and are shown in figure 7.8. A correlation is not observed between the standard deviation and the cantilever beam length in the plotted data in figures 7.8a, 7.8b and 7.8c. However, it can be seen that increasing the exposure duration of the samples to argon ion bombardment decreases the standard deviation across the samples, for cantilever beams of all lengths. Here, the maximum recovery of the deflection of the tip has been 95% for 150μm long cantilever beam, exposed at ions with 250eV energy for 180 seconds, as can be seen in figure 7.8c.

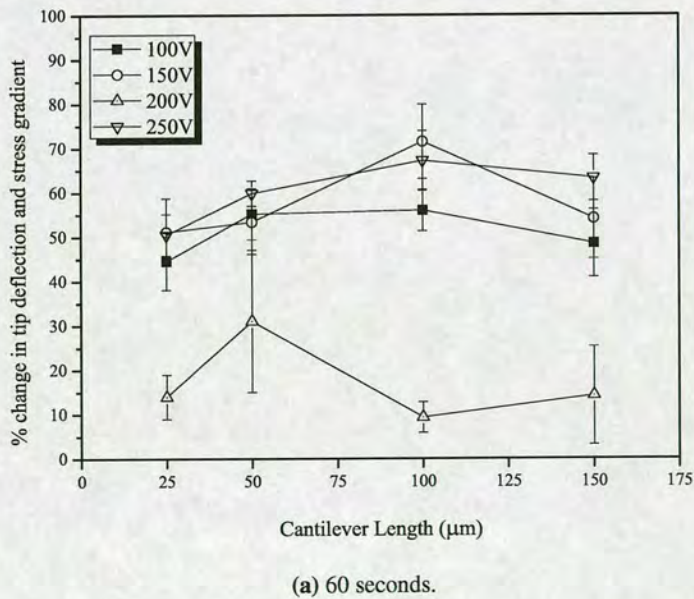
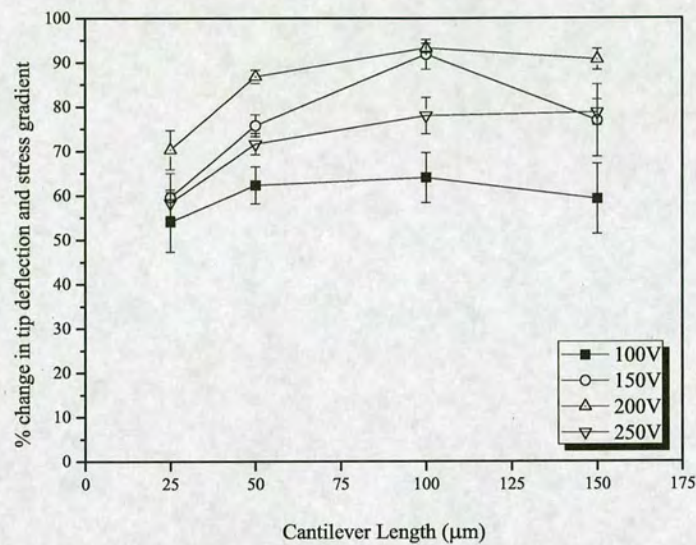
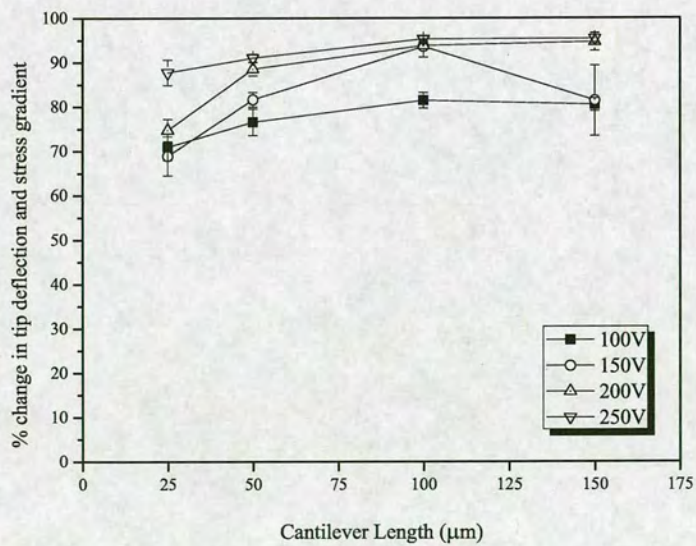


Figure 7.8: Percentage change in the tip deflection and the stress gradient as a function of cantilever length (25μm, 50μm, 100μm, 150μm) after exposure to Ar plasma (100eV, 150eV, 200eV and 250eV).



(b) 120 seconds.



(c) 180 seconds.

Figure 7.8: Percentage change in tip deflection and stress gradient as a function of cantilever length (25μm, 50μm, 100μm, 150μm) exposed to Ar plasma at 100eV, 150eV, 200eV and 250eV.

7.5 Discussion

Thin films that are deposited in the absence of ion bombardment tend to be tensile. However, introducing energetic ion bombardment during the growth process can reduce or even invert the stress state of the material. The structural changes that occur in the target material are believed to depend on the energy of the incident ions, the ion to atom arrival rate ratio, and the type of target material. G. Carter, who reports the simulation findings of various authors, states that incident ions with sufficient energy to overcome the surface potential barrier E_t , penetrate into the material and produce atomic recoils. These recoils may cause densification and defects in the film, reducing or altering the stress state of the material [78]. However, N.A. Marks *et al.* who performed molecular dynamics simulations in order to examine the role of ion bombardment in the growth of carbon films, have shown that stress reduction or alteration can occur even if the incident ions do not penetrate into the target material [79]. Another mechanism that is being reported in the literature to contribute towards the stress modification of materials by energetic ion bombardment, refers to the thermal spikes. According to this theory, as each ion penetrates into the material, it transfers energy to the atoms around the ion damage track. The volume and hence the quench time of these thermal spikes is proportional to the ion energy. The higher the energy, the longer the quench time, allowing more bonding rearrangements in the material and a larger expansion of the affected volume. As time elapses, more ions penetrate the material and a larger portion of the material's volume is treated [78, 80, 81]. The effects of ion bombardment during deposition and post-deposition are the same. However, in the last case stress modification can be achieved only down to the depth of penetration of the incident ions.

Monika Koster and Herbert M. Urbassek have also performed molecular dynamic studies of bombardment of silicon ions in amorphous silicon. The authors proved that stress modification can occur for incident ion energies of 150eV or less. Furthermore, the degree of stress increase or relaxation is dependent on the energy of the incident ions and the bond strength of the atoms in the target specimen [82, 83].

Experimental study of relaxation of internal stress for HfN thin films using Si^+ ion implantation has been reported where energies of the order of keV and low MeV have been employed [84, 85]. He^+ and N^+ ion implantation in the 40-50keV energy regime have been used to relax stress gradients in gold films [86] and argon ions at 500eV have been used to relax stress gradients in polycrystalline silicon thin films [87]. T. Narushima *et al.* have shown that low energy Ar^+ ion bombardment in ICP reactor can induce a compressive stress on the silicon surface and that the

induced surface stress could be recovered by electron irradiation [88].

To investigate the penetration of the Ar^+ ions in the SiC thin film, TRIM simulations have been performed for 10^6 ions. The simulations have shown that the maximum Ar^+ penetration in the a-SiC film is 2nm at 100eV, 2.35nm at 150eV, 2.7nm at 200eV and 3.05nm at 250eV. For such shallow penetration of ions to have such a dramatic effect in the stress relaxation of the a-SiC films, suggests that the stress gradient originates in the surface of the thin film. This confirms the hypothesis that the stress has been induced during the fabrication of the samples using with process 'A'.

The effect of reduced standard deviations in the deflection of the samples with increasing exposure to ion bombardment could be attributed to an initial transient period, where the depth distribution of Ar^+ ions across the subsurface of the material is random. TRIM simulations have shown that as time elapses, the ion distribution in the subsurface approaches the steady state resulting in more uniform treatment of the material. This is reflected in a reduction in the standard deviation of the deflection of the tip of the cantilever beams, as can be seen in figure 7.8.

7.6 Conclusion

The suitability of amorphous silicon carbide thin films for application in MEM devices has been investigated. It has been found that the fabrication process that implements a PECVD SiO_2 mask during the SiC plasma etch, and possibly the removal of the SiO_2 mask using a CF_4/H_2 plasma induces a surface stress in the a-SiC thin film. The induced stress can be relaxed with low energy argon ion bombardment (100eV - 250eV) in ICP reactor. Increasing the exposure duration of the samples to Ar^+ bombardment results in increased stress relaxation uniformity across the samples. Although thermally grown 3C-SiC is an excellent material for MEM applications, as-deposited PECVD a-SiC has not been found to be a reliable material. Therefore, for the fabrication of pressure sensors with silicon carbide membranes thermally grown SiC thin films have been used in chapter 8.

Chapter 8

Absolute pressure sensors with silicon carbide and silicon membranes

In this chapter the fabrication and characterisation of micro-electro-mechanical sensors for measuring the pressure of gases or fluids is presented. The sensors fabricated here implement flexible membranes that deform when a differential pressure is applied across its surfaces. The method used to detect changes in the membrane deformation relies on strain gauges positioned on top of the membranes.

Here we are interested in the fabrication of thin membranes made of silicon carbide. It has been shown previously in chapter 7 that surface stress can be induced in amorphous silicon carbide thin films during the fabrication process, which is not desirable. Therefore, thermally grown silicon carbide has been used in this chapter for the fabrication of flexible membranes. Devices with single crystalline silicon membranes on silicon on insulator wafers have also been fabricated to compare their performance against silicon carbide based pressure sensors. For the detection of the membrane deformation under applied pressure, aluminium and boron doped polycrystalline silicon strain gauges have been fabricated on top of the membranes.

In section 8.1 the sensor design is presented along with the specification of the wafers used here, membrane deflection theory and surface distribution of strains, the chosen strain gauge design here and finally how stresses in the materials that constitute the device affect the deflection of over-constrained thin film membranes. In section 8.2 the fabrication process of the sensors, including aluminium and polycrystalline silicon strain gauges and the deep reactive ion etch that releases the membranes is developed. Finally the micromachined devices are sealed, assembled and tested by General Electric. The device performance results under thermal and pressure loading are presented in section 8.3 and the conclusions are presented in section 8.4.

8.1 Sensor design

The diagram in figure 8.1 shows the cross section of a typical absolute pressure sensor design with strain gauge electro-mechanical transducers.

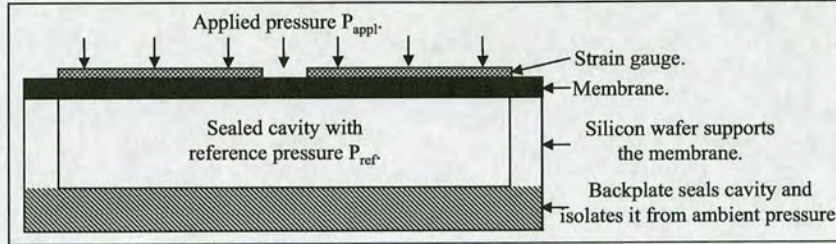


Figure 8.1: Absolute pressure sensor with strain gauges fabricated in this chapter.

These sensors are called absolute because the differential pressure $P_{diff} = P_{appl} - P_{ref}$ that appears across the two surfaces of the membrane is determined by the absolute non-variable reference pressure in the sealed cavity, which is defined in the fabrication process. When differential pressure P_{diff} is applied across the membrane, this is mechanically deformed and the resultant strains modify the resistance of the gauges.

8.1.1 Wafer specification and material parameters

As mentioned at the beginning of this chapter, pressure sensors with silicon carbide and single crystalline silicon membranes with aluminium and boron doped polycrystalline silicon gauges have been fabricated here. The substrate specifications for the silicon carbide, delivered by Novasic [89], and single crystalline silicon based devices are listed in tables 8.1 and 8.2 respectively.

Type	Thickness (μm)	Function
Silicon carbide	2	Sensor membrane
Handle Wafer	425	Support

Table 8.1: 4-inch silicon carbide wafer specification. The SiC has been deposited by Novasic [89].

Similar to the fabrication of cantilever beams in chapters 4 and 5 silicon on insulator wafers (SOI) have been chosen for the fabrication of silicon membranes. In the SOI wafers the presence of buried SiO_2 acts as an etch stop and the handle wafer can be completely etched with bulk micromachining process without affecting the device layer. The buried SiO_2 etch stop

Type	Thickness (μm)	Dopant	Resistivity ($\Omega \cdot \text{cm}$)	Function
Silicon device layer	4 +/- 0.5	Phosphorus	5-10	Sensor membrane
Buried SiO_2	1.5 +/- 0.075	-	-	Etch stop
Silicon handle wafer	380 +/- 5	Antimony	0.02-0.05	Support

Table 8.2: Silicon on insulator wafer specification. The substrate diameter is 4 inches.

layer is removed after this process with a dry etch step that does not attack the silicon in the device layer. For the silicon carbide wafers a separate etch stop layer is not available and the silicon carbide thin film is used to stop the etch.

Because during testing the devices are thermally loaded, it is useful to know the coefficients of thermal expansion (α_{CTE}) that constitute the devices, which is defined by equation 8.1.

$$\alpha_{CTE} = \frac{dv}{V \times dT} \quad (8.1)$$

where dv is the change in the volume of the material for change dT in temperature. The coefficients of thermal expansion, Young's moduli and gauge factors (where applicable) of the materials that constitute our devices have been listed in table 8.3.

Type	Coefficient of thermal expansion α_{CTE} (K^{-1})	Young's modulus (GPa)	Gauge Factor
LPCVD polycrystalline silicon	$\leq 4.4 \times 10^{-6}$ [90]	160 [90]	10-40* [23, 91, 92]
3C-SiC	3.1×10^{-6} [93]	370 [73]	-
Single crystalline silicon	2.3×10^{-6} [52]	136 [94]	-
Thermal SiO_2	0.5×10^{-6} [53]	-	-
Aluminium	0.5×10^{-6} [52]	69.6 [95]	~ 2.7 [96]
PECVD SiO_2	-4×10^{-6} [90]	42 [90]	-

*Polycrystalline gauge factor depends on deposition and boron doping conditions.

Table 8.3: Coefficients of thermal expansion of materials used in the pressure sensors.

Before proceeding to the fabrication of the devices, membrane theory relevant to our application and the chosen strain gauge designs are presented in section 8.1.2.

8.1.2 Membrane deflection theory and strain gauge design

To define the strain gauges on membranes for optimal sensitivity, the stress distribution that appears on the surface of the membrane during mechanical deformation must be investigated. For the pressure sensors here, the membranes are subjected to uniform pressure and are said to be in pure bending. From Timoshenko's theory of plates and shells, the deflection w of clamped plate under application of uniform load is given by equation 8.2 [97].

$$w = \frac{P}{64D}(\alpha^2 - r^2)^2 \quad (8.2)$$

where P is the applied pressure in Pascal units, r is the radius of the plate and a is the distance from the center of the plate. At the center of the plate $r = 0$ and at the edge $r = \alpha$. The quantity D replaces the flexural rigidity EI in the case of beams and for plates it is expressed by equation 8.3.

$$D = \frac{Eh^3}{12(1 - \nu^2)} \quad (8.3)$$

where E is the modulus of elasticity, h is the membrane thickness and ν is Poisson's ratio. The flexural rigidity expresses the ease of membrane deformation to applied pressure. The circumferential ϵ_c and radial ϵ_r strains are given by equations 8.4 and 8.5 respectively.

$$\epsilon_c = -\frac{3Pa^2(1 - \nu^2)}{8Eh^2}\left[1 - \left(\frac{r}{\alpha}\right)^2\right] \quad (8.4)$$

$$\epsilon_r = -\frac{3Pa^2(1 - \nu^2)}{8Eh^2}\left[1 - 3\left(\frac{r}{\alpha}\right)^2\right] \quad (8.5)$$

Using equations 8.2, 8.4 and 8.5, the deflection of clamped membrane and the resultant strains on the top side of the membrane have been calculated and are represented graphically as a function of $\frac{r}{a}$ in figure 8.2.

The deflection profile from the membrane center toward the clamped edge can be seen in the top part of the graph and the resulting circumferential and radial strains on the top side of the membrane can be seen in the lower part of the figure. It is observed in the lower graph that the circumferential strain on the top membrane side is always negative (tensile), it is minimal at the membrane edge and maximal at the center of the membrane. The radial strain is positive (compressive) at the center of the membrane and reduces to zero at $r = 0.577\alpha$. From $r = 0.577\alpha$ to $r = \alpha$ at the clamped edge of the membrane, the radial strain strain becomes negative (tensile).

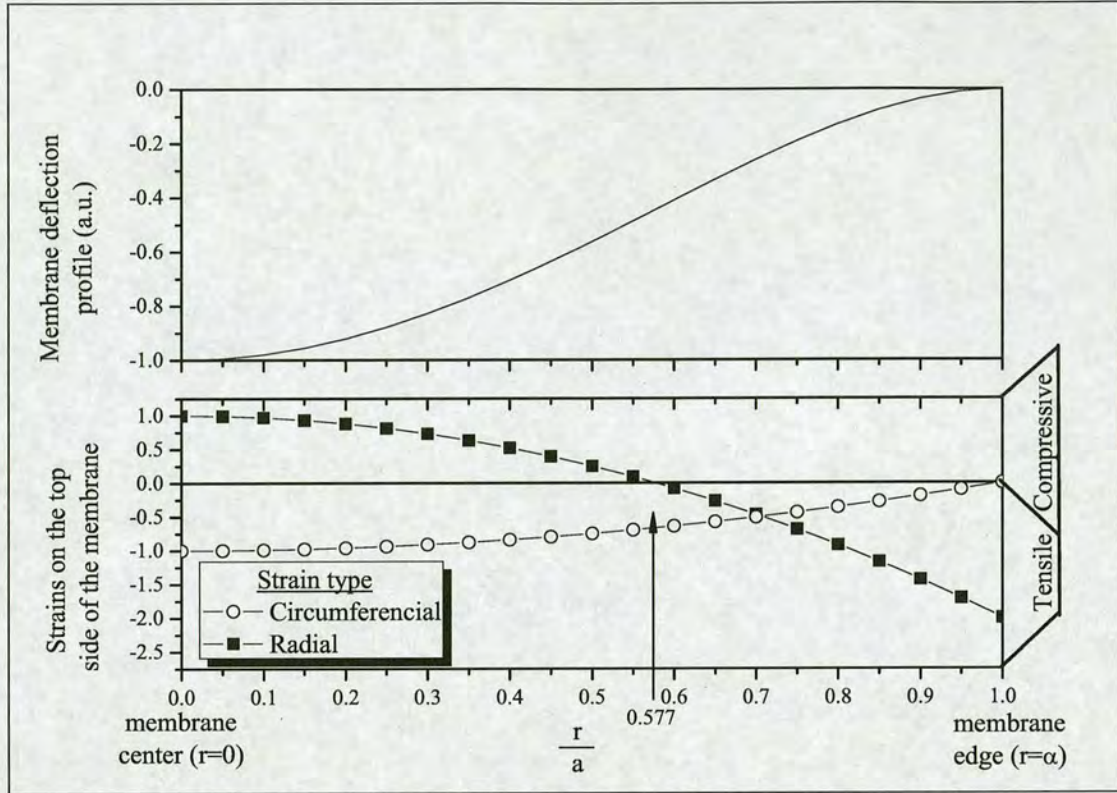


Figure 8.2: Top part: clamped membrane deflection profile. Low part: resulting strains on the top side of the membrane.

The gauge factor K , a quantity that describes the gauge sensitivity to applied strain, has been given previously in equation 2.8 (chapter 2, page 18), which states that it is defined by $K = \frac{1}{\epsilon} \frac{\Delta \rho}{\rho}$, where ϵ is the applied strain and $\Delta \rho$ is the fractional change in resistivity of the gauge. Solving for fractional resistance change we deduce $\frac{\Delta \rho}{\rho} = K\epsilon$ and it can be seen that for given gauge factor K the fractional change in resistance is proportional to applied strain, hence the average applied strain $\epsilon_{average}$ along the gauges should be maximized to achieve optimal performance.

Using the convention that compressive and tensile strain is positive and negative respectively, the average absolute strain along a gauge that experiences both compressive and tensile strains along different portions of its length can be described as $|\epsilon_{average}| = |\epsilon_{compressive} - \epsilon_{tensile}|$. The absolute strain $|\epsilon_{average}|$ sensed by the gauge is maximized when $\epsilon_{compressive}$ or $\epsilon_{tensile}$ is zero, ie. when the strain gauge is subject only to compressive or only to tensile strain. This should be taken into consideration at the design phase of the devices.

By using the strain distributions from figure 8.2 and the conclusions from last paragraph, the

gauges can be configured for optimal sensitivity. Figure 8.3(i) shows four possible optimized gauge arrangements, where each gauge would sense only tensile or only compressive strain. Strain gauge designs (i.1) and (i.2) are subject to radial tensile strain only. In gauge design (i.3) the semiconductor gauge is subject to compressive radial strain only and in design (i.4) the semiconductor gauge is subject to circumferential tensile strain only.

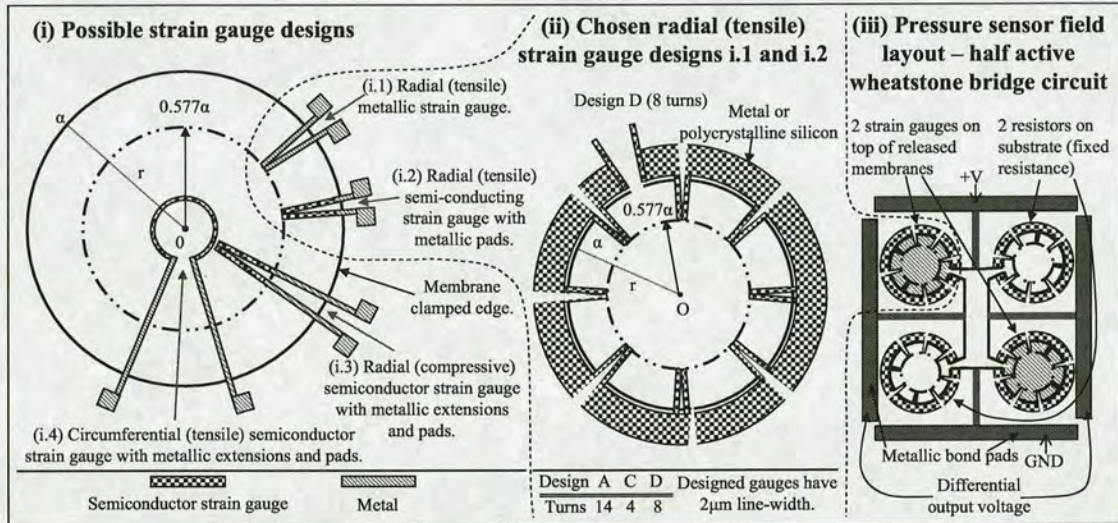


Figure 8.3: (i) four possible strain gauge designs on circular membrane, (ii) the chosen and designed gauge layout here, and (iii) the pressure sensor field layout with 2 strain gauges and 2 fixed resistors configured in half-active Wheatstone bridge circuit.

To allow for the fabrication of devices with either metallic or semiconductor strain gauges with minimal number of masks, designs (i.1) and (i.2) seen in figure 8.3(i) that have similar layouts have been selected. Figure 8.3(ii) shows the layout of designed strain gauges for the pressure sensors here. These gauges would be subject only to radial tensile strain if pressure has been applied on the surface of this page, causing the membrane to bend away from the reader. In the chosen design, the gauges can be made by deposition and patterning of either polycrystalline silicon or metal. Three layouts 'A', 'C' and 'D' with 14, 4, and 8 turns respectively have been designed and the line-width of the gauges has been $2\mu\text{m}$ in all designs. Two different materials will be used for the fabrication of the strain gauges: a) pure aluminium and b) polycrystalline silicon deposited with the LPCVD method and doped with boron by implantation.

In figure 8.3(iii) the pressure sensor field layout can be seen, where on each die two circular strain gauges would be positioned on released membranes and two additional circular fixed resistors would be used to fabricate a closed half-active Wheatstone bridge circuit. The circuit

is based on configuration (c) shown in table 2.3, chapter 2, page 23.

8.1.3 Stress in membranes

Stresses in micro-electro-mechanical systems are usually undesirable because they may cause significant mechanical deformation that would not allow proper device operation. However, thermally induced stresses are desirable in a special category of MEM systems called thermal actuators. In our devices, the three main stress sources are listed in the next three paragraphs:

a) after a high temperature thin film deposition/growth on substrate, mismatch in the coefficients of thermal expansion of the materials implies that they contract at different rates when cooled to room temperature and, due to traction at the interface of the films, stresses appear. Once the thin film membranes have been released by deep etching of the substrate beneath the micromembranes, traction between the microstructures and the substrate is locally eliminated and residual stress in the thin films is relaxed, causing mechanical deformation of the structures. In under-constrained structures (ie. cantilever beams), relaxation of an axial stress causes elongation or shrinking of the free end when the stress is compressive or tensile respectively. In over-constrained structures (ie. clamped beams and membranes) relaxation of residual stress results in buckling or cracking of the structures, depending on whether the stress in the thin film is compressive or tensile respectively.

b) although the stress in defined and released over-constrained thin film microstructures may not be present at room temperature, temperature induced stresses are caused when mismatches in coefficients of thermal expansion between the thin film and the substrate result in dissimilar expansion/contraction in the volume of the materials. For example if the thin film microstructures expand faster than the substrate that supports them, compressive stresses will appear across the microstructures. Because the structures have been released the stresses will be relaxed instantaneously causing mechanical deformation.

c) in the case of released bimorph or trimorph microstructures that are constituted by two or three stacked thin films respectively, differences in the coefficients of thermal expansion of the films introduce stress gradients across the thickness of the structures when the temperature is modified. As seen in chapter 7 stress gradient may cause significant mechanical deformation of released microstructures. Although this principle is used to fabricate devices that use thermally induced stress gradients for actuation of released structures, it may be an undesirable effect in

other applications.

To summarize, the three aforementioned main stress sources in fabricated, over-constrained microstructures are: a) residual thin film stresses from the deposition stage, b) thermally induced stress due to mismatch of coefficients of thermal expansion between the released thin film microstructures at the boundaries with the supporting substrate, and c) thermally induced stress gradients across the thickness of bimorph/trimorph microstructures due to mismatches in coefficients of thermal expansion between the thin films that constitute the bimorph/trimorph microstructures. Depending on the device design one, two, or all of these stress sources may act coinstantaneously and cause deformation of the structures.

R. Arya *et al.* have fabricated thermally actuated trimorph SiO_2/Si /metal bistable membranes [52]. These membranes, which are unstable in the flat state, take advantage of differences between coefficients of thermal expansion of the films to introduce thermally induced stress gradients that cause the membranes to snap between two buckled (up and down) mechanically stable states. The critical snapping temperatures have been as low as 50-60°C. Hsu *et al.* have also researched thermally actuated mechanically stable bimorph membranes with deposited and patterned films of various materials on top of the membranes that result in temperature induced continuous membrane deflection [98]. Using finite element modeling, the authors have shown that by varying: a) the boundary conditions of bimorph silicon membranes by etching [of the membranes], b) the selected films that are deposited on top of the membrane, and c) the defined layout of the deposited films by etching, the membrane bimorph structures can bend continuously in either up or down direction. For clamped membranes with electrodes located at the outer region of the membrane, similar to our design shown in figure 8.3(ii), the structures deform in the downward direction when heated.

To summarise the previous paragraph, it has been found in the literature that temperature induced stresses in the bimorph/trimorph membrane structures may cause snapping or continuous deformation of the membranes. Finite element modeling simulations have not been performed here to predict the membrane behavior to variations in the ambient temperature. Next, the device fabrication starting from the strain gauges on the substrate surface is developed.

8.2 Device fabrication

As mentioned at the beginning of this chapter, both silicon carbide and single crystalline silicon membranes are fabricated here on substrates with 4 inch diameter, with metallic aluminium and boron doped polycrystalline silicon strain gauges. Next the strain gauges are fabricated on the surface of the substrates.

8.2.1 Aluminium strain gauge fabrication

Aluminium strain gauges are unreliable, have poor sensitivity in comparison to semiconductor gauges and show erratic sensitivity in their gauge factor [96]. For these reasons the use of aluminium in MEM sensors normally function as circuit interconnects only. However, as first attempt aluminium strain gauges have been fabricated with the process shown in figure 8.4.

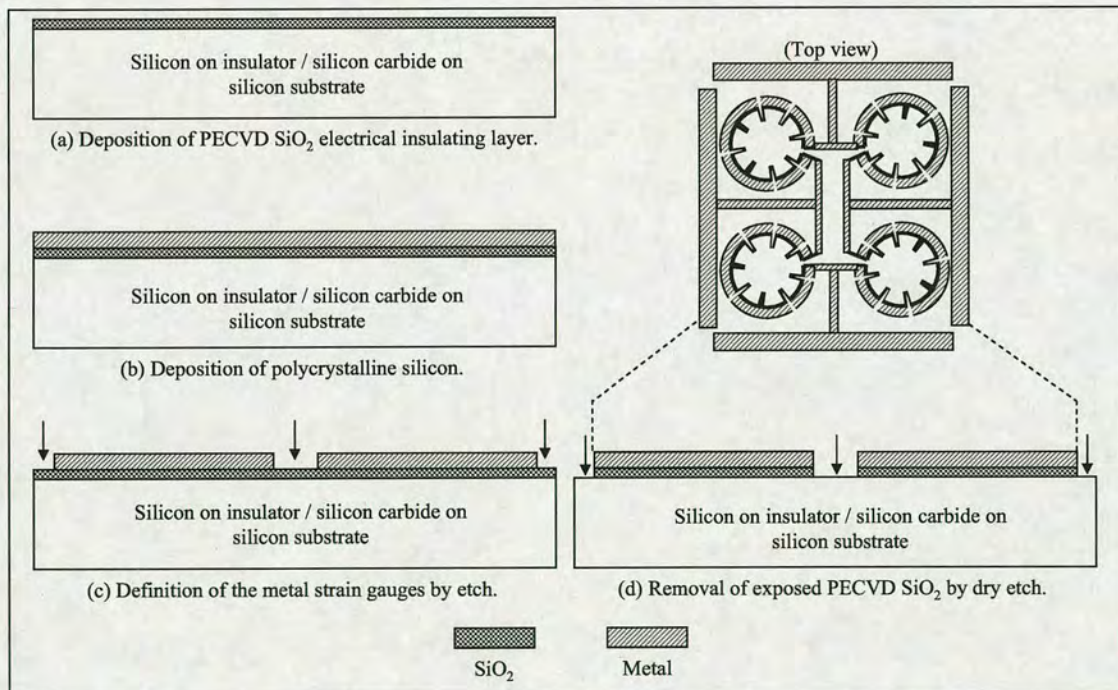


Figure 8.4: Fabrication of aluminium strain gauges on insulating SiO_2 .

Initially 170 nm thin SiO_2 film has been deposited by the PECVD method (fig. 8.4a) to provide electrical insulation between the conducting substrate and the metallic strain gauges. Next, 0.5 μm thin aluminium film has been deposited by magnetron sputtering (fig. 8.4b), patterned photolithographically and defined in heated (50°C-70°C) Rockwood wet etchant (fig. 8.4c)

revealing the underlying SiO_2 film. Finally the exposed SiO_2 has been removed by a dry etch step in CF_4/H_2 plasma (fig. 8.4d).

8.2.2 Polycrystalline silicon strain gauge fabrication

In addition to low performance metallic gauges, doped polycrystalline silicon gauges that are used commonly as strain gauges due to their enhanced piezoresistive properties have also been fabricated. Here polycrystalline silicon gauges have been fabricated with the process shown in figure 8.5. 170 nm thin SiO_2 film has been deposited by the PECVD method (fig. 8.5a). Next,

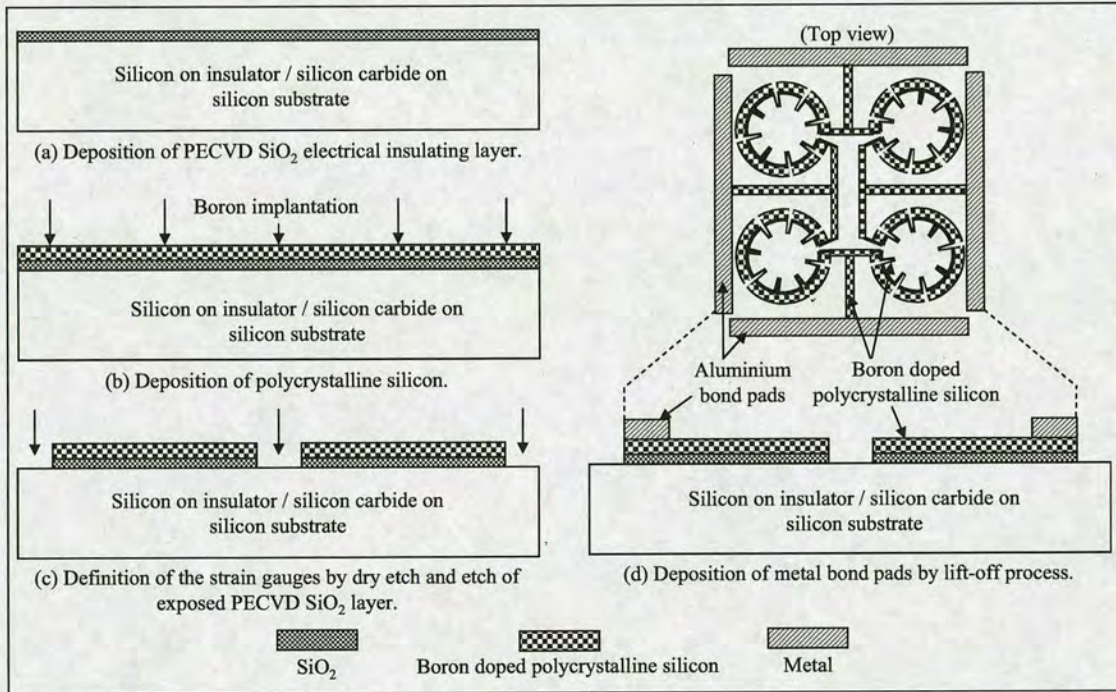


Figure 8.5: *Fabrication of boron doped polycrystalline silicon strain gauges with insulating SiO_2 .*

0.3 μm thin polycrystalline silicon film has been deposited by the low pressure chemical vapor deposition method at 620°C in silane (SiH_4) and the wafer has been implanted with boron at Ion Beam Services at 50keV ion energy and 10^{15} atoms/ cm^2 ion dose (fig. 8.5b), followed by boron activation at 1000°C for 30 minutes in N_2 environment. The wafers have been patterned photolithographically and the polycrystalline silicon has been etch anisotropically in CF_4/H_2 plasma. The etch has been continued to remove the exposed SiO_2 (fig. 8.5c). To add bonding capability to the devices, 0.5 μm thin pure aluminium film has been deposited by magnetron

sputtering and patterned with lift-off process (8.5d). The lift-off has been performed using LOR5B and positive imaging resist, according to the process shown in chapter 6, figure 6.3a-d, pp. 89. Finally a sinter step at 435°C for 30 minutes in N₂/H₂ environment has been performed to produce ohmic interfacial contacts between boron doped polycrystalline silicon and the aluminium pads. After the strain gauge fabrication, the bulk micromachining process of the handle wafers for the release of the membranes has been investigated.

8.2.3 Bulk micromachining by deep reactive ion etch

Since circular membranes are fabricated here, bulk micromachining of the handle wafers by wet crystallographic etch is not suitable as only rectangular patterns can be defined with this method and dry bulk micromachining process is used for the removal of the bulk silicon and definition/release of the membranes. A new Bosch recipe 'B' that uses fixed pressure control valve, where the work pressure during etch and passivation cycles is controlled by the gas flows has been implemented. The Bosch process details can be found in appendix B, table B.3.

8.2.3.1 Investigation of the deep etch bosch recipe

To investigate the etch profile of the process, 525μm thick trial wafer with 150nm thin PECVD SiO₂ layer on the polished side and circular patterned features in 15μm thick SPR220.7 photoresist on the unpolished side have been prepared. After completion of the process the wafer has been diced across the etched cylinders causing shattering of the SiO₂. The remaining SiO₂ film has been removed in hydrofluoric acid. Next, the samples have been inspected in the scanning electron microscope and selected micrographs of etched cylinder with 300μm diameter are shown in figure 8.6. The Bosch recipe etch characteristics are listed in table 8.4.

Bosch process	Silicon etch rate (μm/cycle)	Sidewall angle (at 300μm depth)	Silicon/SPR220.7 photoresist etch selectivity
B	0.658	1.81°	67.56

Table 8.4: *Characteristics of the Bosch etch recipe 'B'.*

Because the electrically insulating silicon oxide film has been present on the bottom of the wafer during the deep etch process, positive ions have been accumulating on the thin film causing build up of electrical charge. Due to this electrical field, incoming ions have been deflected toward the sidewalls resulting in the notching effect, as can be seen in figure 8.6b. Furthermore,

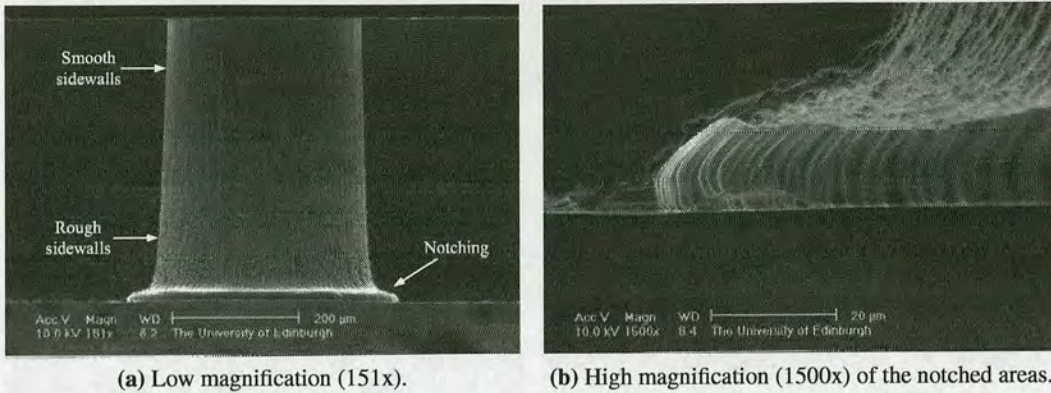


Figure 8.6: Scanning electron images of: a) a 300 μm wide deep etched cylinder, and b) the notching effect due to the non-conducting SiO_2 that has been present during the etch process.

it can be seen in the scanning electron micrograph, in figure 8.6a, that the sidewall surface becomes rougher as the deep etch advances through the substrate. This could also be attributed to the ionic deflection towards the silicon sidewalls arising from the presence of the aforementioned electric field. This effect would also be expected to occur in the SOI wafers at the interface between the buried SiO_2 etch stop layer and the handle wafer. For devices with non-conducting silicon carbide membrane electrical charge would also accumulate on the SiC thin film and cause notching at the boundary of the film with the silicon substrate.

8.2.3.2 Definition and release of membranes by bulk etching

After the trial investigation of the deep etch micromachining process, the wafers with defined aluminium and boron doped polycrystalline strain gauges have been prepared for the deep etch. On the silicon on insulator wafers, the thermal polished SiO_2 on the backside of the handle wafers has been removed in CF_4/H_2 plasma. Next the backside of both SOI wafers and the silicon on carbide on silicon wafers have been patterned photolithographically with 15 μm thick SPR220.7 resist to prepare the wafers for the bulk etch micromachining step. For the silicon carbide devices the silicon substrate has been completely deep etched with Bosch recipe 'B' to release the SiC thin film. For the SOI wafers the silicon substrate has been deep etched with Bosch recipe 'B' to reveal the buried SiO_2 . Subsequently the buried SiO_2 layer in the silicon on insulator wafers has been removed by an additional dry etch in CF_4/H_2 plasma. The remaining photoresist on the wafers has been removed in fuming nitric acid, followed by rinsing in de-ionized water and blow drying in with N_2 gun. The diagram in figure 8.7a shows the

fabricated silicon membranes with boron doped polycrystalline silicon and aluminium metallisation on SOI wafers, where the notched regions from the ionic bombardment on the silicon sidewalls during the deep reactive ion etch process are indicated. In figure 8.7b the diagram of released silicon carbide membranes is illustrated. The notched regions formed in the deep reactive ion etch are indicated by dashed circles. Furthermore, the trimorph polycrystalline Si/PECVD SiO₂/(Si or SiC) membranes are clearly indicated.

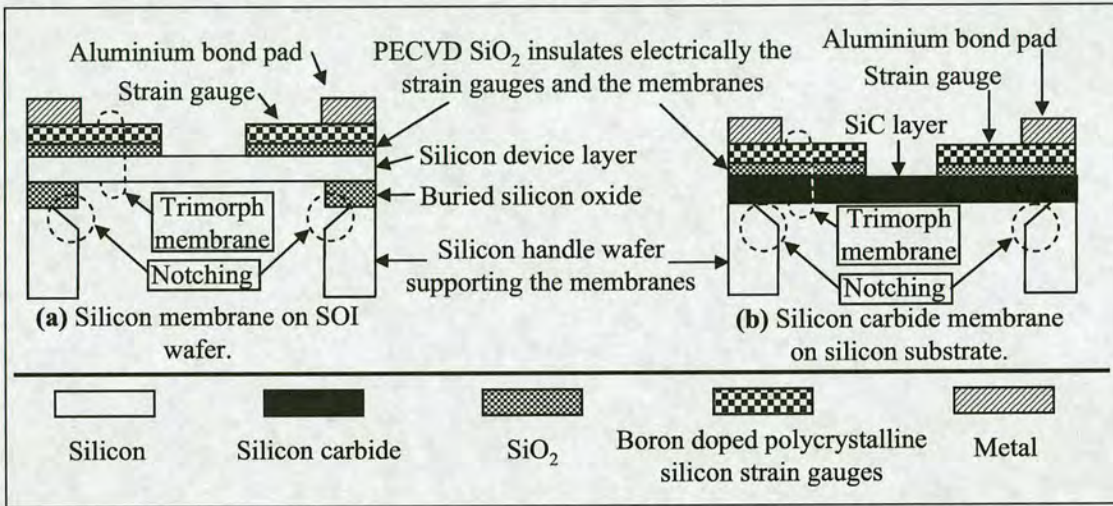


Figure 8.7: Polycrystalline Si/PECVD SiO₂/(Si or SiC) trimorph membranes, defined and released by deep reactive ion etching of the silicon substrate.

Optical micrographs of micromachined membranes with strain gauges are shown in figure 8.8. Figure 8.8a shows device D.500 (strain gauge design D with 8 turns and 500 μ m diameter silicon carbide membrane) where the top left and bottom right diaphragms have been released. The released, transparent to light silicon carbide membranes can be seen clearly in the optical image in figure 8.8b where backlight illumination has been used. The optical micrograph (Nomarski) of silicon membrane on SOI wafer with 500 μ m diameter and gauge design 'D' can be seen in figure 8.8c, where minor buckling of the membrane is observed. This minor deflection is attributed to stress gradients between the polycrystalline Si/PECVD SiO₂/Si films from the fabrication stage. Similar deformation has been observed for the SiC based trimorph structures. A released SiC membrane with 200 μ m diameter and strain gauge design 'C' can be seen in figure 8.8d, where it is observed that the membrane boundary is not uniform due to the roughness in the silicon substrate sidewalls from the deep reactive ion etch process. The line-width of the gauges has been 2 μ m for all designs and the fabricated membranes have diameters of 100 μ m, 200 μ m, 300 μ m, 400 μ m, 500 μ m, 600 μ m, 900 μ m and 1200 μ m.

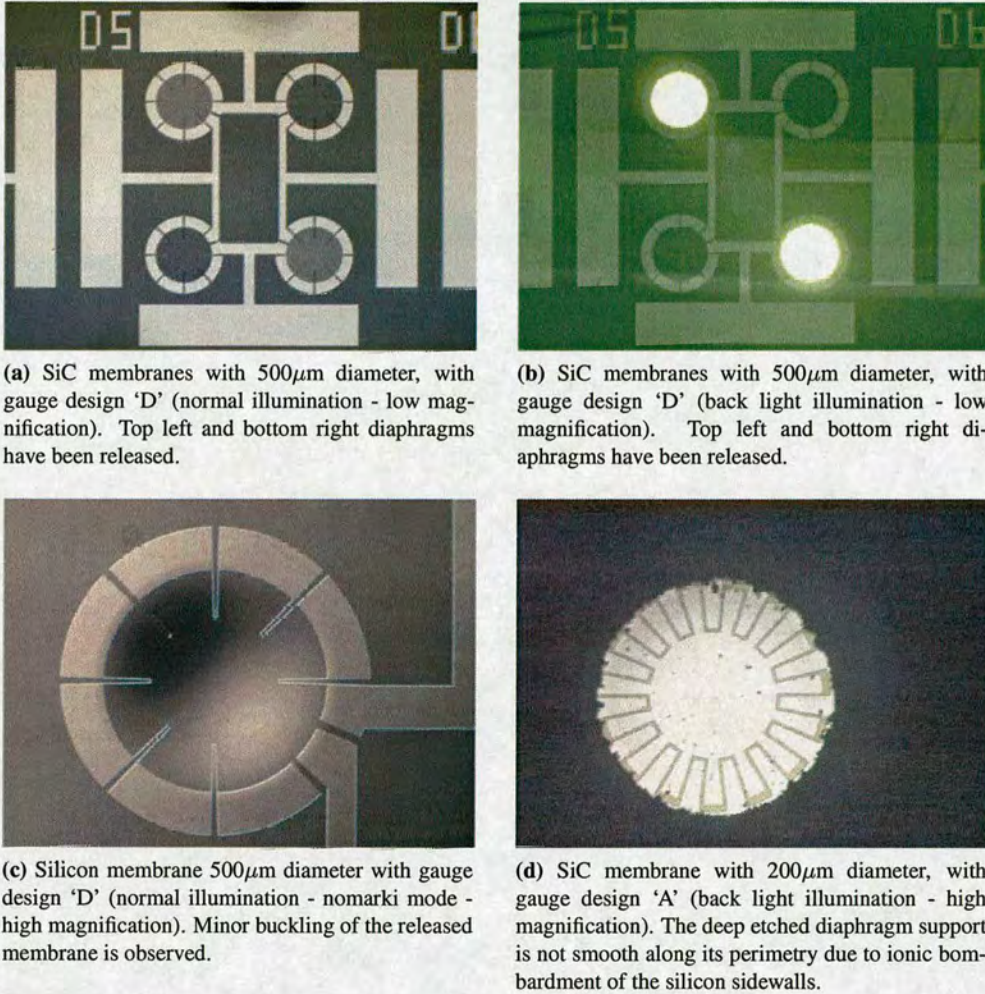


Figure 8.8: Optical microscope images of the top view of micromachined sensors with aluminium gauges.

8.2.4 Device sealing and assembly

The micromachined wafers have been shipped to the sensing division of General Electric for final processing which includes substrate bonding with glass backplate to define the sealed cavity, wafer dicing, and device assembly.

The diagrams in figure 8.9a,b illustrate the cross sections of Si and SiC based devices after bonding of the glass backplate with anodic bonding, which is carried out in vacuum environment. After anodic bonding the fabrication process has been complete and the wafers have been diced in die with 3.2mm² area. The photograph in figure 8.9c shows the die of silicon carbide

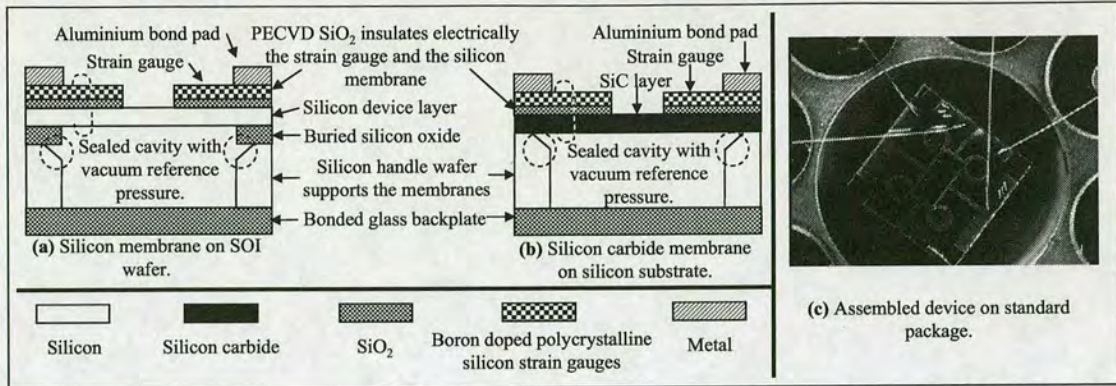


Figure 8.9: Fabricated pressure sensors: a) before, b) after the anodic bonding process, and c) after assembly in standard pressure sensor package.

pressure sensor with aluminium gauges assembled by General Electric in a standard package prior to device testing.

8.3 Device performance

After assembly, the performance of packaged devices has been tested by General Electric in a rig where the applied pressure and temperature can be varied. Three different test configurations have been implemented to investigate the performance of the devices: a) variable thermal and pressure loading, b) variable thermal loading at two fixed pressure (0mBar and 700mBar) loads, and c) variable pressure loading at room temperature. The electrical probing of the half-active Wheatstone bridge circuits during testing has been setup to produce a positive change in the differential output signal when membranes bend toward the sealed cavity due to applied pressure. Obviously when the membranes bend away from the cavity the circuit will produce a negative change in the differential output voltage. Furthermore, the devices may be affected by thermal loading which may cause mechanical deformation of the membranes. This can be observed from variations in the offset voltage of the half-active Wheatstone bridge circuits. During the tests Wheatstone bridge offset voltage cancelation circuits have not been used, so that both the differential output signal due to applied pressure and the possible variation in the Wheatstone bridge offset voltage due to membrane deformation arising from thermal stresses, has been recorded.

8.3.1 Device performance under thermal and pressure loading

In this test 7 runs have been performed. At the beginning of each run, the pressure has been set initially to 0mBar, the temperature has been set at the desired level (-40°C to 130°C) and subsequently the pressure has been ramped to 700mBar. The device output has been recorded constantly throughout the runs. The parameters for each run (temperature, pressure) can be seen in figure 8.10, in the first two rows where the applied pressure and temperature are identical across all three columns. The output of the devices has been plotted in the next four rows where the identification (gauge design and membrane diameter in μm) of each tested device is indicated on its corresponding plot. The results for Si membranes with aluminium gauges are listed in column (i), for Si membranes with boron doped polycrystalline Si gauges in column (ii), and for SiC membranes with boron doped polycrystalline Si gauges in column (iii).

8.3.1.1 Performance of silicon membranes with aluminium gauges

The response of silicon membranes with aluminium gauges can be seen in figure 8.10, column (i). Devices A.400 and A.600 barely show a differential output signal as response to applied pressure in each run, but the Wheatstone bridge offset voltage appears responsive to temperature variations. Devices C.400 and C.900 show pressure induced electrical output in each run, but the offset voltage of the devices varies erratically. Generally the output signals of silicon membranes with unreliable aluminium gauges has been inconsistent, as expected, and conclusions on the response of the membranes to thermal and pressure loading cannot be drawn.

8.3.1.2 Performance of silicon membranes with polycrystalline silicon strain gauges

The response of silicon membranes with boron doped polycrystalline silicon gauges can be seen in figure 8.10, column (ii). Apart from the device C.400 that has erratic behavior, devices A.400, A.900 and C.900 show consistent response to the applied pressure for runs no.1-5 and no.7, where the temperature for these runs ranges between -40°C to 80°C but does not exceed 80°C. For run no.6, where the temperature has been ramped to 130°C, a sharp change in the offset voltage of the devices has been observed. For devices A.400 and C.900 the sharp change in the signal output has been positive, and for device A.900 the output has been negative. This indicates that critical temperature exists between 80°C to 130°C where the trimorph (polycrystalline Si/PECVD SiO₂/Si) membranes snap erratically in either up or down direction due to

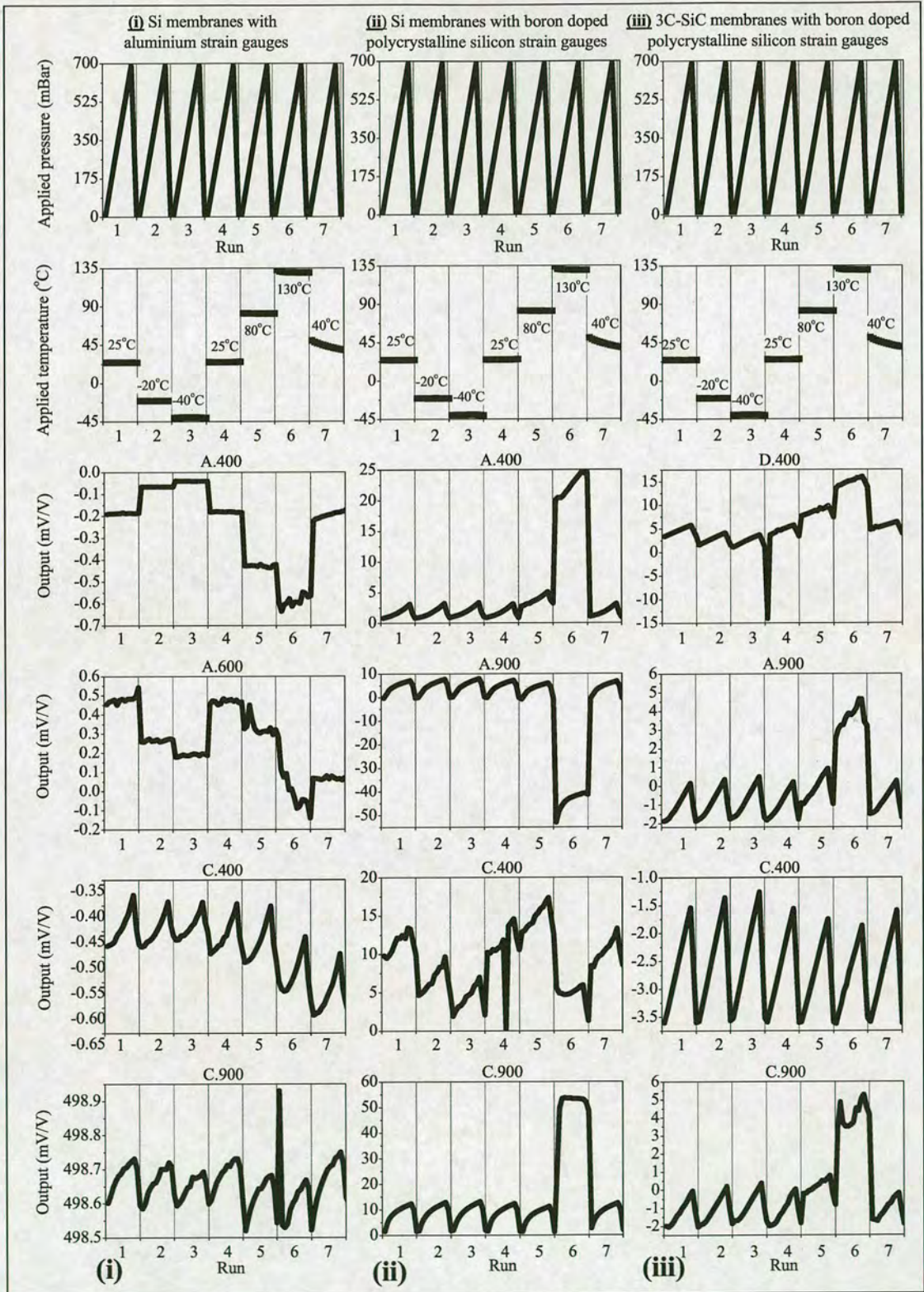


Figure 8.10: Sensitivity of devices: (i) Si membranes with aluminium gauges, (ii) Si membranes with polycrystalline silicon gauges, and (iii) 3C-SiC membranes with polycrystalline Si gauges for thermal (-40 to 130°C) and pressure (0-700mBar) loading.

stress gradients, causing the observed sharp change in the output offset voltage of the Wheatstone bridge circuit. As mentioned previously in section 8.1.3, thermally induced snapping of trimorph membranes has been observed by R. Arya *et al.* [52].

8.3.1.3 Performance of silicon carbide membranes with polycrystalline silicon strain gauges

The response of silicon carbide membranes with boron doped polycrystalline silicon gauges can be seen in figure 8.10, column (iii). It is observed that for device D.400 the half-active Wheatstone bridge offset voltage across the seven runs is positively correlated to the applied temperature, indicating temperature induced continuous deformation of the released trimorph membranes. In addition to temperature modulated offset voltage, the device shows response to the applied pressure in each run. Temperature induced continuous deformation of bimorph membranes has also been observed by Hsu *et al.* [98], as mentioned previously in section 8.1.3. However, the same continuous deflection is not observed for devices A.900 and C.900 where snapping occurs at high temperature run no.6. Device C.400 has been the best performer and is the only device where the Wheatstone bridge offset voltage is not modified by the temperature across all runs implying the released trimorph membrane for this device neither deforms continuously or snaps in response to temperature variations. The device output in response to applied pressure is clearly seen. Furthermore for device C.400, it is observed that an increase in temperature results in reduced maximum signal output at 700mBar and a decrease in temperature results in increased maximum signal output at 700mBar. This implies that the device sensitivity is thermally modulated and is negatively correlated to the ambient temperature.

8.3.1.4 Comparison of device performance

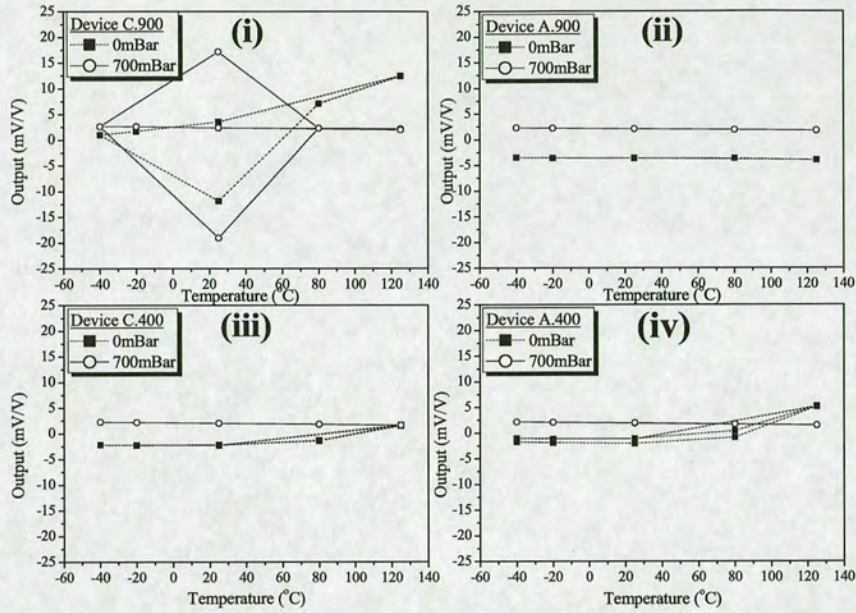
As discussed earlier, the performance of aluminium gauges has been poor and the results are inconclusive. Most devices (A.400, A.900 and C.900) made of silicon membranes with boron doped polycrystalline silicon gauges have shown stable performance for runs no.1-5 and no.7, where the temperature ranges between -40°C and 80°C . It has been observed that critical temperature exists between 80°C to 130°C , in run no.6, where the trimorph polycrystalline Si/PECVD SiO_2/Si membranes snap erratically in either upward or downward direction.

For devices made of SiC membranes and boron doped polycrystalline silicon gauges, the per-

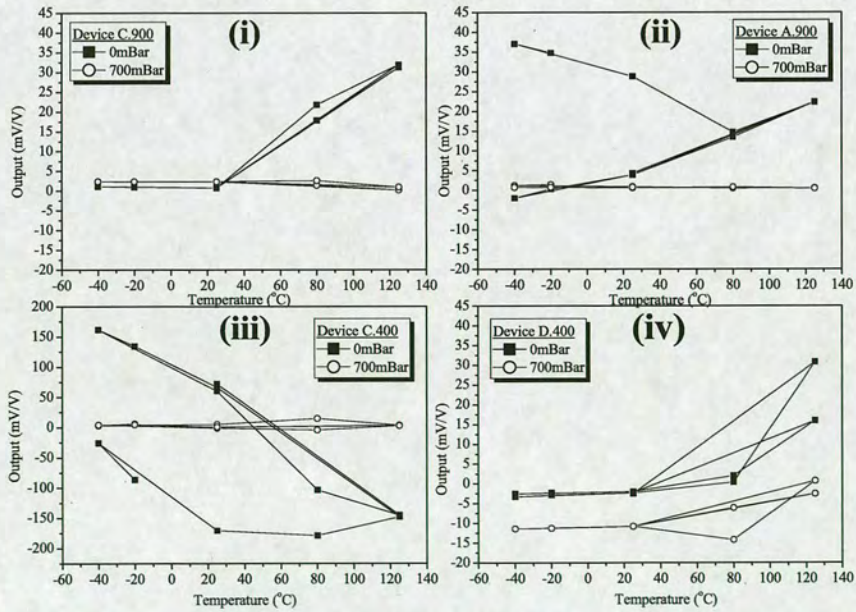
formance has not been coherent. Device D.400 has shown continuous membrane deflection in response to temperature variations, whereas devices A.900 and C.900 exhibit snapping behavior at critical temperature level between 80°C-130°C. Only the device C.900 has shown a stable performance across all 7 runs and elevated temperatures up to 130°C. The overall performance of the devices in these tests has not been stable.

8.3.2 Device performance under thermal loading at fixed pressure levels

In these tests, initially the applied pressure in the rig has been set to 0mBar at room temperature. The temperature has been cycled between -40°C and 130°C, while the device output has been recorded. Next the pressure has been set to 700mBar and the temperature has been cycled again between -40°C and 130°C. Because the devices with aluminium strain gauges have performed poorly in previous tests, these have not been re-tested here. The response of silicon membranes can be seen in figure 8.11a, and the response of SiC membranes with boron doped polycrystalline Si gauges can be seen in figure 8.11b. As mentioned before in this chapter, the devices respond to variations in the ambient temperature due to mismatches in the coefficients of thermal expansion between its constituting materials that result in stresses. Here the effects of these thermal stresses are investigated. Overall in these tests both Si and SiC based devices have demonstrated a more stable signal output at temperature variations when 700mBar pressure has been applied at room temperature prior to cycling the temperature. In contrast, the output of the devices has been erratic during temperature cycling for 0mBar applied pressure. This indicates that the trimorph membranes are sensitive to initial test conditions and do not demonstrate a stable performance. The best performer has been the crystalline silicon based device A.900 (fig.8.11a(ii)) which does not seem to be affected by temperature loading at any pressure level. However, it should be noted that the same device in previous tests (fig.8.10, column (ii), A.900) has shown snapping behavior at 130°C. Generally the behavior of devices under thermal loading has been unstable.



(a) Single crystalline silicon membranes (SOI wafers).



(b) 3C-SiC membranes.

Figure 8.11: Hysteresis curves of: a) single crystalline Si trimorph membranes and b) 3C-SiC trimorph membranes for temperatures ranging from -40°C to 130°C at 0 and 700mBar applied pressures.

8.3.3 Device performance under pressure loading at room temperature

Since the devices have been unstable at thermal loading, additional tests have been carried out at room temperature in order to gain an insight in the sensitivity of the devices to applied pressure. The performance of Si and SiC based devices to applied pressure range from 0mBar to 700mBar can be seen in figure 8.12 (i) and (ii) respectively.

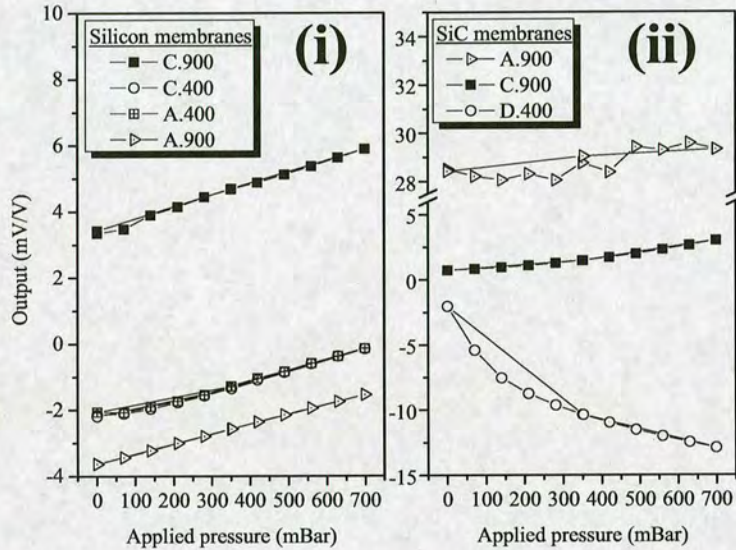


Figure 8.12: Hysteresis curves of: (i) single crystalline Si and (ii) 3C-SiC membranes, at 0-700mBar applied pressure range in room temperature.

The single crystalline silicon membranes demonstrate better stability compared to silicon carbide devices. In the SiC set, only device C.900 shows reasonably linear output-pressure performance, whereas devices A.900 and D.400 show inconsistent results. The sensitivity of devices with linear output-pressure characteristics are listed in table 8.5, where it can be seen that for the tested devices the Si based sensor C.900 is slightly more sensitive by 0.38×10^{-3} (mV/V/mBar) compared to equivalent SiC device. However, to draw statistically significant results a larger set of devices would have to be tested. Although the Si based devices appear to be slightly more sensitive compared to their SiC counterparts, the results are not statistically significant and it would not be wise to generalize on these results.

Type	Device identification	Device sensitivity (mV/V/mBar)
Silicon	C.900	3.63×10^{-3}
	C.400/A.400	2.84×10^{-3}
	A.900	2.98×10^{-3}
3C-SiC	C.900	3.25×10^{-3}

Table 8.5: Sensitivity of Si and SiC based devices at room temperature at 0-700mBar pressure range.

8.4 Conclusion

In this chapter single crystalline Si circular membranes on SOI wafers and 3C silicon carbide circular membranes on silicon substrates have been fabricated by bulk deep reactive ion etching of the substrates. On each device field with 3.2mm^2 area, two released membranes have been fabricated and metallic aluminium and boron doped polycrystalline silicon strain gauges have been positioned on top of the release membranes. In addition to the two strain gauges, two fixed resistors have been fabricated on each field to produce closed half-active Wheatstone bridge circuits that provide differential voltage in response to membrane bending due to thermally induced stresses and applied pressure.

The micromachined devices have been shipped to General Electric where the backside of the substrates has been bonded anodically with a thick glass backplate to isolate the etched cavities from the ambient pressure and define a reference pressure. The devices have been diced and assembled into standard pressure sensor packages for testing purposes.

Three tests have been carried out with different combinations of thermal and pressure loads to investigate the performance of the devices. Initially in section 8.3.1 the devices have been loaded both thermally and with pressure. The devices with silicon membranes and aluminium strain gauges have shown erratic electrical output due to the poor quality of the metallic gauges and the results have not been discussed further. Silicon membranes fabricated on silicon on insulator wafers with insulating PECVD SiO_2 and polycrystalline Si gauges have shown snapping behavior at critical temperatures between 80°C to 130°C . Such membrane behavior has been observed in trimorph structures by R. Arya *et al.* [52]. Here snapping behavior is believed to be due to differences in the coefficients of thermal expansion between the silicon membrane (2.3×10^{-6}) and the buried thermal silicon oxide (0.5×10^{-6}). As temperature is elevated the over-constrained silicon membranes expand faster compared to the underlying thermal buried

SiO₂ layer and compressive stresses appear. Because the membranes have been released, the stresses relax instantaneously causing the membranes to buckle when the temperature exceeds a critical level. In addition, stress gradients appear across polycrystalline Si/PECVD SiO₂/Si trimorph membrane structures due to differences between the coefficients of thermal expansion of the thin films ($\leq 4 \times 10^{-6}$ for polycrystalline Si, -4×10^{-6} for PECVD SiO₂, 2.3×10^{-6} for Si), which combine with the aforementioned compressive stress that appears across the over-constrained membrane at elevated temperatures. The weighed contribution of each stress source (compressive and gradient) to the snapping membrane behavior is not known. The stress analysis for devices based on single crystalline silicon membranes, also applies to devices with SiC membranes. The mismatch between the coefficients of thermal expansion between SiC (3.1×10^{-6}) and its underlying silicon (2.3×10^{-6}) substrate is significant and would also result in compressive stresses across the over-constrained SiC membranes at elevated temperatures. The SiC based devices have also been unstable to thermal and pressure loading and have exhibited continuous or snapping deflection in response to thermal loading.

In section 8.3.2 the devices have been subject to thermal cycling between -40°C and 130°C at two fixed pressure levels at 0mBar and 700mBar. When thermally loaded at 0mBar applied pressure, the membrane behavior has been unstable and is in agreement with the results obtained from the tests summarised in the previous paragraph. However, when the devices have been thermally loaded with application of constant 700mBar pressure on the surface of the membranes, the stability has shown remarkable improvement. This implies that the membrane performance to thermal loading depends on the initial pressure conditions.

Finally, in section 8.3.3 pressure loading tests have been carried out at room temperature where it has been found that single crystalline silicon membranes consistently possess linear output-pressure characteristics in contrast to SiC membranes, and Si based devices are slightly more sensitive by 0.38×10^{-3} (mV/V/mBar) compared to their SiC counterparts. However, due to the limited number of devices tested and the generally unstable device performance from previous tests, these results are not statistically significant and it would not be wise to generalize on these tests alone.

Although the work carried out in this chapter aimed to produce absolute pressure sensors with silicon membranes and 3C-SiC membranes for harsh conditions (high temperature and high pressure), the performance of the devices has been found to be inconsistent and unstable. The main problems are thought to exist in mismatches between coefficients of thermal expan-

sion between the materials that constitute the devices, causing stresses and unpredictable device behavior under thermal loads. Matching the membrane material with its underlying supporting substrate would eliminate a thermally induced stress source and would be the first step in improving the reliability of the devices.

Chapter 9

Conclusion

The main body of this thesis (chapters 2-6) has presented the fabrication process development for a bio-inspired micro-electro-mechanical air flow sensor. For this purpose, conventional microfabrication techniques have been exploited. Although the MEM sensor has not been fully developed in this thesis, significant contribution in developing the sub-components of the sensor has been made.

Minor part of the thesis (chapters 7-8) has been dedicated to the investigation of suitability of amorphous silicon carbide for application in MEMS. Pressure sensors with silicon and silicon carbide membranes fabricated using conventional microfabrication techniques have been tested under thermal and pressure loads.

The main conclusion from each section in this thesis is discussed.

9.1 Development of bio-inspired MEM air flow sensor

The MEM air flow sensor would be integrated with neuron LSI circuit and robot and would assist researchers at the School of Informatics to study the behavior of the cricket modulated by air flow. The detailed specifications of the MEM air flow sensor have been given in chapter 2 and main points of the specification state that micro-electro-mechanical artificial hair cells with hair of variable length should be fabricated and should produce electrical signal modified by air flow.

Previous work on bio-inspired MEM systems [11–14, 16] has been reviewed in chapter 1. A sensor design similar to the approach taken by Zhifang Fan *et al.* [11] would meet the specifications here and therefore, has been chosen. This sensor design consists of: a) Wheatstone bridge circuits made of p-type boron doped regions in n-type single crystalline silicon, integrated with patterned metallisation, b) silicon cantilever beams that are integrated with the full-active Wheatstone bridge circuits, c) out of plane flaps of variable length that are integrated at the free end of the silicon cantilever beams.

9.1.1 Characterisation of boron implantation and integration of boron doped microfeatures with metallisation

Experimental chapters (3-6) begin with the characterisation of p-type boron implantation in single crystalline silicon and integration of the implanted microfeatures with metallisation in chapter 3.

The distribution profile of the implanted and activated boron in single crystalline silicon has been characterised using ion mass spectroscopy (SIMS), TSuprem4 simulations and 4-point sheet resistance electrical measurements. The simulated and electrical measurements have been found to be in good agreement with the experimental results obtained from SIMS analysis. The implanted microfeatures (Wheatstone bridges) have been integrated with TiN/Ti and Al-1%Si metallisations. Ohmic Al-1%Si – boron doped microfeature contacts have been established after sintering at 435°C and therefore, aluminium with one percent silicon has been chosen as metallisation for the MEM system.

9.1.2 Integration of electrical circuits with silicon microcantilever beams

Next step has been the integration of Wheatstone bridge/metallisation circuits with released silicon microcantilever beams.

In chapter 4 the first attempt to integrate full-active Wheatstone bridge circuits with micromachined silicon cantilever beams on silicon on insulator wafers has been made. The Wheatstone bridge (p-type microfeatures/metallisation) electrical circuits and cantilever beams have been fabricated in the device layer of the SOI wafers. To release the structures, the handle wafer beneath the predefined cantilever beams has been removed by wet or dry bulk micromachining. The wet approach has been found to not be reliable as opposed to the dry etch approach that has been successfully implemented to release the cantilever beams. However, integration of full-active Wheatstone bridge circuits with released cantilever beams has been partly successful. Although mechanical deformation of released structures induced Wheatstone bridge differential output voltage, the devices did not have linear current-voltage circuit characteristics, exhibited low sensitivity to air stimulation, and therefore did not meet the specifications and could not be integrated with the LSI circuit.

In an attempt to address the aforementioned issues, the MEM devices have been redesigned in chapter 5 to meet the specifications. The redesigned devices included half-active Wheatstone

bridge circuits for integration with second generation microcantilever beams that implement improved stress concentration regions, aiming to improve the device sensitivity to air flow. An additional feature in the new devices is the inclusion of multilevel metallisations that would reduce the number of final bonding pads on the die to 72, in comparison to 192 bonding pads that would be necessary if a single metallisation had been implemented. To achieve metallisation in two levels, planarisation of the substrate's surface after the deposition of the first patterned metallisation layer has been necessary. The planarisation with spin-on-glass dielectric has been characterised and successfully implemented.

New devices have been fabricated to include half-active p-type boron doped Wheatstone bridge microfeatures, integrated with two-level metallisation and micromachined, dry etched, cantilever beams. Electrical testing has revealed non-conducting electrical circuits, implying electrical discontinuity at some point in the circuits. The devices have been investigated both electrically and in the scanning electron microscope, where failure of the second metallisation level, due to poor adhesion of aluminium at the sidewalls of the vias, has been confirmed. Including a titanium adhesion layer as part of the second metallisation, prior to deposition of aluminum, is thought to solve the current problem.

9.1.3 Development of the plastic deformation magnetic assembly process

The third component of the MEM sensor consists of out of plane flaps for integration at the free end of released silicon cantilever beams. To achieve out of plane flaps as the final structures, metallic seed layer is deposited on a sacrificial layer and nickel-iron permalloy is electrodeposited on top of the metallic seed layer. To achieve out of plane deformation of the composite seed layer – Ni-Fe permalloy flaps, the sacrificial layer is removed to release the structures and the released flaps are exposed to magnetic field. Under the influence of magnetic flux torque appears across the Ni-Fe permalloy causing out of plane deformation of the composite seed layer – Ni-Fe permalloy flaps.

A PECVD SiO_2 sacrificial layer for etch in hydrofluoric acid has been investigated. The release of overlying nickel seed layer has been successfully implemented. Subsequently the morphology of the electrodeposits by SEM, chemical composition by X-ray photoelectron spectroscopy and wafer electrodeposition uniformity by profilometry have been characterised.

Finally the plastic deformation magnetic assembly process has been demonstrated by wet and

vapor hydrofluoric acid etch of the PECVD SiO₂ layer and release of the overlying composite nickel seed layer – Ni-Fe permalloy structures. Although the wet release has shown low yield results, sacrificial etch of SiO₂ in Memsstar's hydrofluoric acid vapor tool has resulted in process with 100% yield.

Plastic deformation magnetic assembly has been achieved by deformation of the structures at the location of the hinge. However, after out of plane deformation the hinges are not rigid and further strengthening, while the flaps are being bent out of plane, is necessary to ensure permanent out of plane deformation.

9.1.4 Further work

Although the work carried out here has not produced MEM air sensors integrated with the neuron LSI, as proposed initially, significant contribution has been made in developing the various sub-components that constitute the MEM air sensors.

The integration of Wheatstone bridge/metallisation circuits with second generation micromachined silicon cantilever beams has been partly successful. The remaining issue to be tackled is the electrical continuity of the second metallisation layer at the location of the vias. This would be achieved by the addition of titanium adhesion layer as part of the second metallisation, prior to deposition of the top aluminium layer.

The development of out of plane flaps has been successfully demonstrated using the PDMA technique on trial wafers. To allow integration of the flaps with the cantilever beams, a method that strengthens the hinge of the structures to allow out of plane permanent deformation of the structures at all times must be employed. This can be achieved by the use of a magnet to deform the flaps out of plane, while additional nickel is deposited on top of the deformed hinges in electro-less solution.

Finally, for the fabrication of the final devices, the PDMA method must be integrated with the Wheatstone bridge/metallisation circuits and silicon cantilever process. This requires the design of additional photolithographic masks for the alignment of composite seed layer – Ni-Fe permalloy structures with the silicon microcantilever beams on SOI wafers. The complete fabrication diagram for the wind sensor is illustrated in appendix C.

9.2 Application of silicon carbide in MEM pressure sensing systems

In this part of the thesis, the suitability of amorphous silicon carbide as structural material for MEM devices has been investigated. Furthermore, thermally grown 3C-SiC has been used for the fabrication of membranes.

9.2.1 Amorphous SiC for application in MEMS

Amorphous silicon carbide thin films deposited by the PECVD method on a silicon substrate have been used to fabricate microstructures by employing dry RIE micromachining techniques. Compressively stressed PECVD SiO₂, low stressed and tensilely stressed PECVD SiN, and tensilely stressed metallic nichrome have been patterned and used as masking materials during the RIE etch and release of *a*-SiC microcantilever beams. After fabrication of the microstructures and removal of the masking material, deflection of the structures has been observed. The degree of microstructure deflection varied according to the masking material, implying fabrication induced surface stress modification of the *a*-SiC thin film. It has been found that the surface stress in the silicon carbide films could be relaxed by low energy (100-250eV) argon ion bombardment in ICP reactor. Because the surface stress state of *a*-SiC could be modified by the fabrication procedure, which is not desirable, thermally grown 3C-SiC has been used for the fabrication of membrane based pressure sensors.

9.2.2 Fabrication of membrane based pressure sensors

The sensors fabricated here implement released flexible circular membranes that deform when differential pressure is applied across them.

Two types of membranes have been fabricated here: i) membranes made of single crystalline silicon device layer on SOI wafers and ii) membranes made of thermally grown 3C-SiC thin films deposited on a silicon substrate. The membranes have been defined and released by DRIE of the silicon substrate in both cases. The method used to detect pressure induced membrane deformation involves aluminium and boron doped polycrystalline gauges strain gauges positioned on top of the membranes.

After fabrication, the devices have been shipped to General Electric where the micromachined

cavities have been sealed by anodic bonding of glass plate on the backside of the silicon substrates, thus creating isolated cavities with fixed reference pressure. Next the devices have been assembled and tested by the sensing division of General Electric. To test the performance of the devices, pressure (0-700mBar) and thermal loads (-40-130°C) have been applied.

As expected, the aluminium strain gauges have shown poor performance, as opposed to polycrystalline silicon strain gauges have been found to be reliable detectors of membrane deformation. It has been found that the devices exhibit unstable performance when loaded thermally and for the majority of devices, critical temperature exists between 80°C and 130°C where the membranes exhibit snapping behavior.

Although the work carried out in this chapter aimed to produce absolute pressure sensors with silicon membranes and 3C-SiC membranes for harsh conditions (high temperature and high pressure), the performance of the devices has been found to be inconsistent and unstable. The main problems are thought to exist in mismatches between coefficients of thermal expansion between the materials that constitute the devices, causing stresses and unpredictable device behavior under thermal loads.

Chen *et al.* have demonstrated recently that capacitive pressure sensors consisting only of silicon carbide, eliminate mismatches in thermal coefficients of expansion and can operate at high temperatures and pressures [99].

9.2.3 Further work

Limiting factor in the performance of the devices has been the fact that thermally induced stresses arise from differences in the coefficients of thermal expansion between the membrane and its supporting substrate. To eliminate these stresses and improve device reliability at high temperatures, the released membrane and its supporting substrate should be made of the same material, as Chen *et al.* [99] have shown recently.

9.3 Publications

Some of the work carried out in this thesis has been published in relevant journals. The journal publications are listed in chronological order:

P. Argyrakis, P. McNabb, A. J. Snell, and R. Cheung, "Relaxation of process induced surface stress in amorphous silicon carbide thin films using low energy ion bombardment", *Applied Physics Letters*, vol. 89, 034101, 2006.

P. Argyrakis, A. Hamilton, B. Webb, Y. Zhang, T. Gonos and R. Cheung, "Fabrication and characterization of a wind sensor for integration with a neuron circuit", *Microelectronic Engineering*, vol. 84, pp. 1749-1753, 2007.

Y. Zhang, A. Hamilton, R. Cheung, B. Webb, P. Argyrakis and T. Gonos, "Integration of Wind Sensors and Analogue VLSI for an Insect-Inspired Robot", *Artificial Neural Networks Conference (IWANN)*, 4507, 438-446, June 2007, Best Paper Award.

R. Cheung, P. Argyrakis, "Micro-scale Sensors based in Silicon Carbide and Silicon", *Proceedings of the I MECH E Part C Journal of Mechanical Engineering Science*, vol. 222, pp. 19-26, 2008.

M. Pozzi, A.J. Harris, J.S. Burdess, P. Argyrakis, K.K. Lee, R. Cheung, G.J. Phelps and N.G. Wright, "Design, Fabrication and Testing of 3C-SiC Sensors for High Temperature Applications", *Proceedings of SPIE*, vol. 6800, pp. 68001S 1-10, 2008.

Additional work is being carried out to characterise further the vapor hydrofluoric acid etch process implemented in the PDMA method, which will be submitted for publication in a relevant journal in the near future.

Appendix A

Silicon elastic and piezoresistive properties

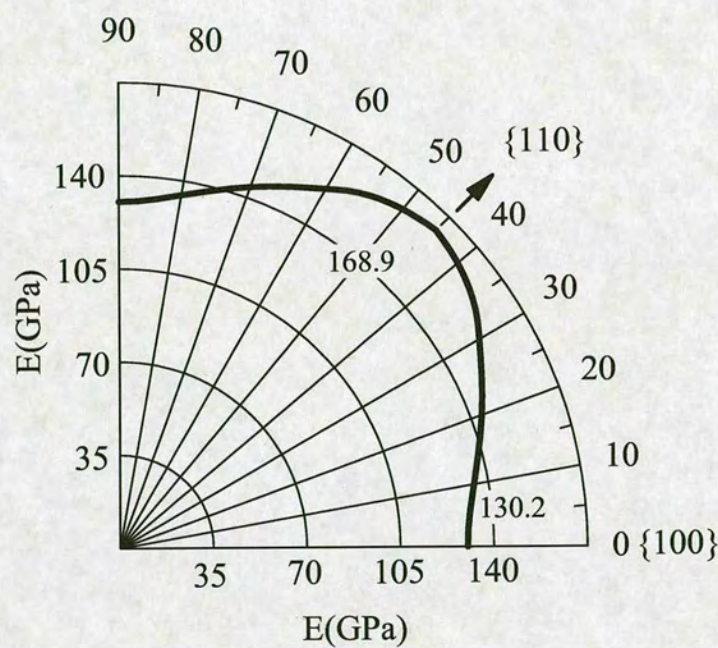


Figure A.1: Elastic properties of silicon. Reproduced from [100].

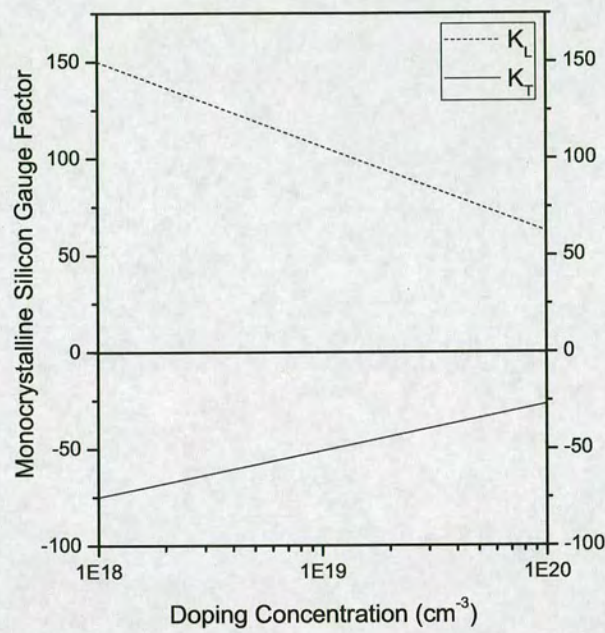


Figure A.2: Longitudinal and transverse gauge factors for single crystalline silicon. Reprinted from [23].

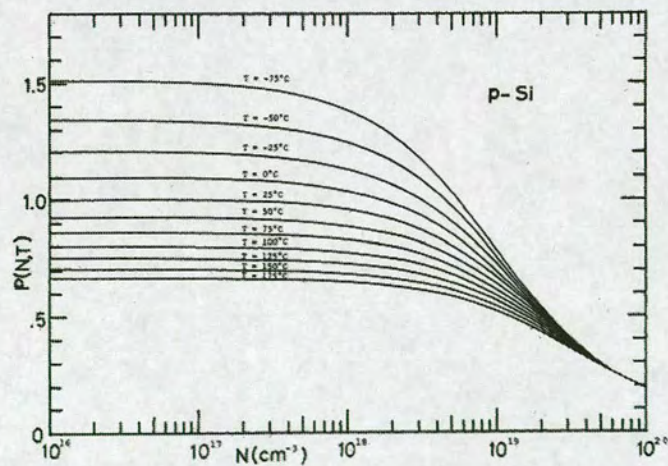
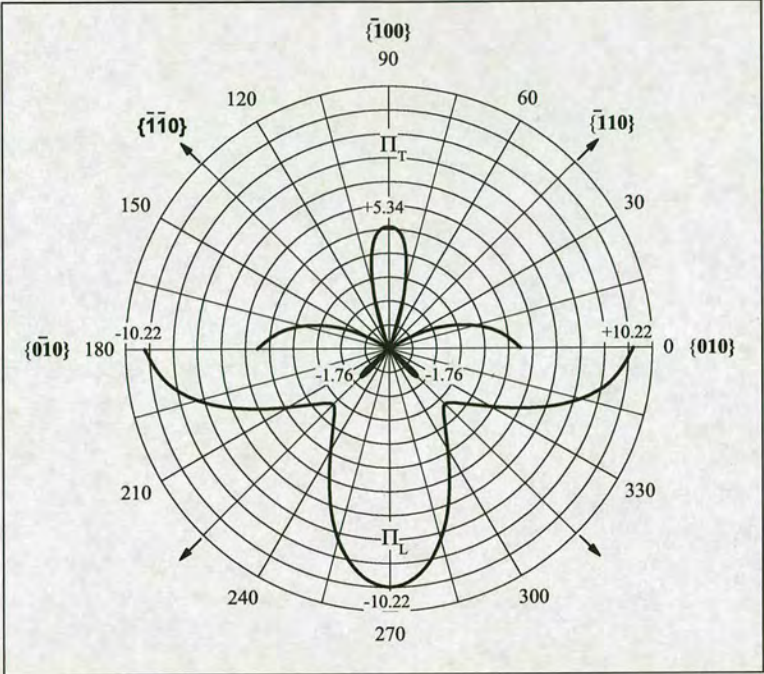
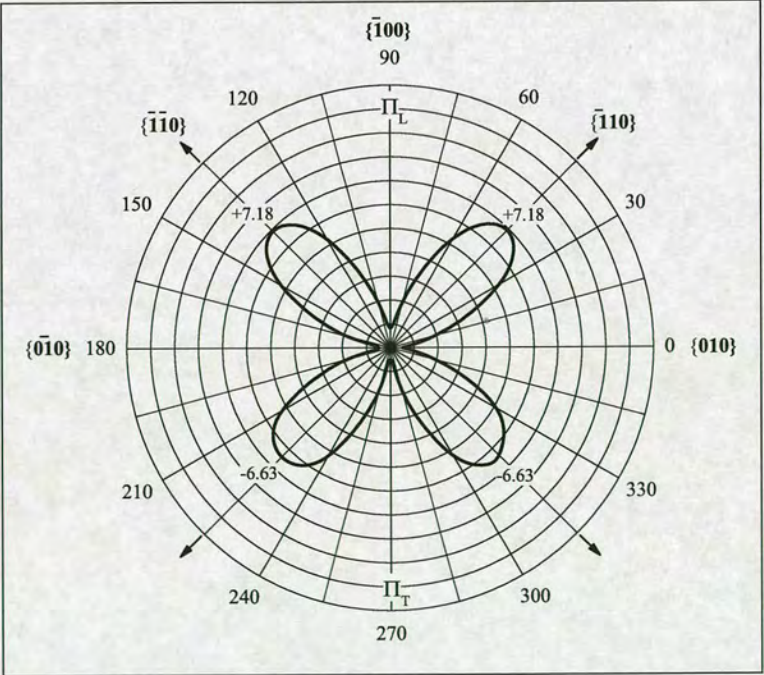


Figure A.3: Piezoresistance factors for p-type silicon. Taken from [25].



(a) N-type



(b) P-type

Figure A.4: Piezoresistive coefficients for silicon in the $\{100\}$ plane, at room temperature. Reproduced from [25].

Appendix B

Thin film deposition and plasma etch conditions

Material	Gas Flows (sccm)			Pressure (mT)	Power (W)	Frequency	Stress
	N ₂	N ₂ O	SiH ₄				
SiO ₂	390	1420	10	900	30	13.56MHz	Compressive
	390	1420	12	550	60	380KHz	Tensile
SiN	N ₂	NH ₃	SiH ₄				
	1960	20	40	900	30	13.56MHz	Tensile
	1960	55	42	550	60	380KHz	Compressive

Table B.1: Deposition conditions for the PECVD Surface Technology Systems (STS) tool. The temperature deposition for all conditions is 300°C.

Material	Gas flows (sccm)		Pressure (mT)	Power (W)
	N ₂	Ar		
Titanium	-	50	15	1000
Titanium Nitride	22	28	10	1000

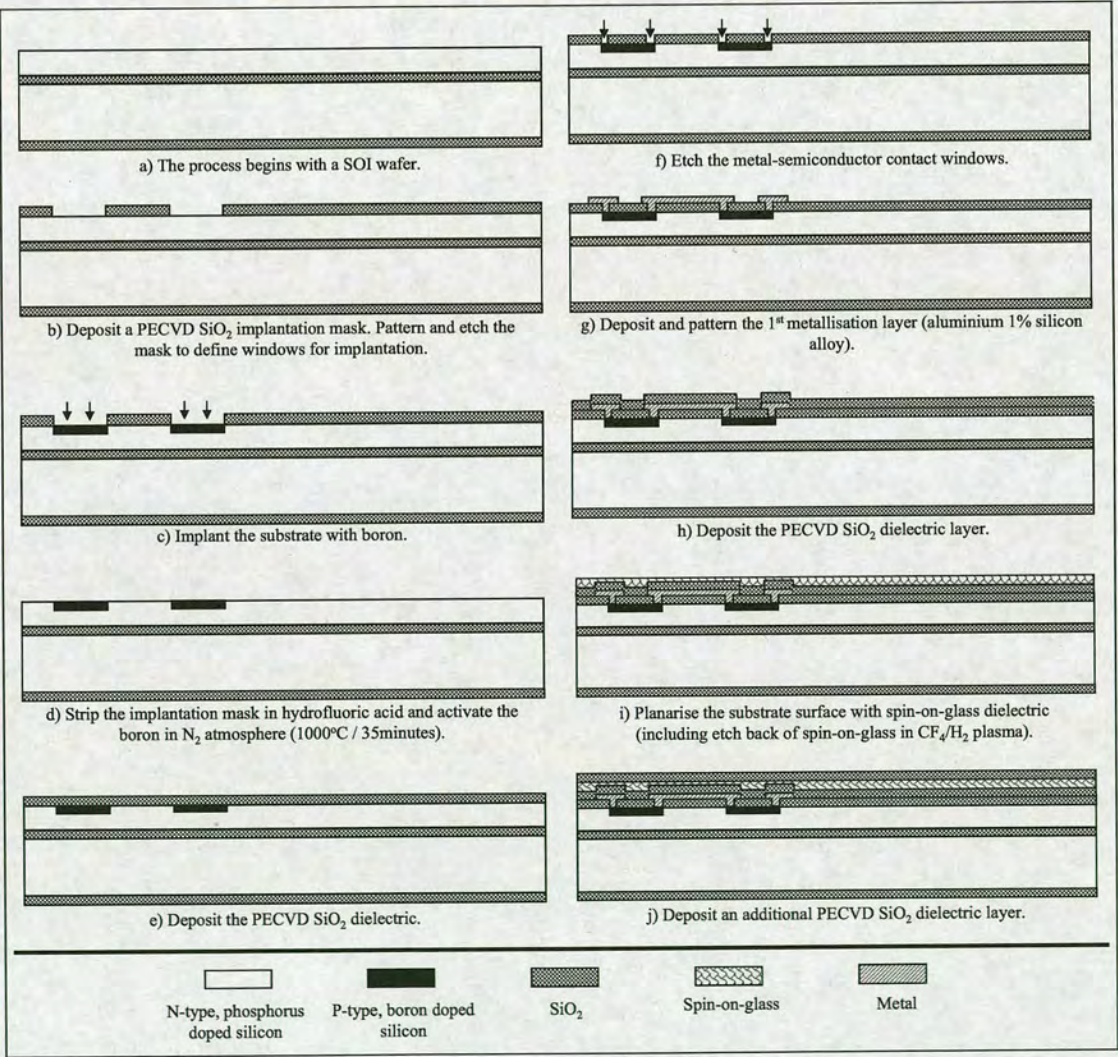
Table B.2: Deposition conditions for the Oxford Plasma Technologies magnetron sputter system.

Recipe	Variable APC*	Cycle	Gas flows (sccm)			Coil Power (W)	Platen Power (W)	Pressure (mT)	Cycle Duration (sec)
			SF ₆	O ₂	C ₄ F ₈				
Recipe A	Yes	Passivation Etch	-	-	85	600	0	25	7
			130	13	-	600	15	25	13
Recipe B	No	Passivation Etch	-	-	85	600	0	26	8
			130	13	-	600	12	20	12

Table B.3: Bosch recipes details for use in the Surface Technology Systems (STS) inductive coupled plasma reactor (*Automatic Pressure Control).

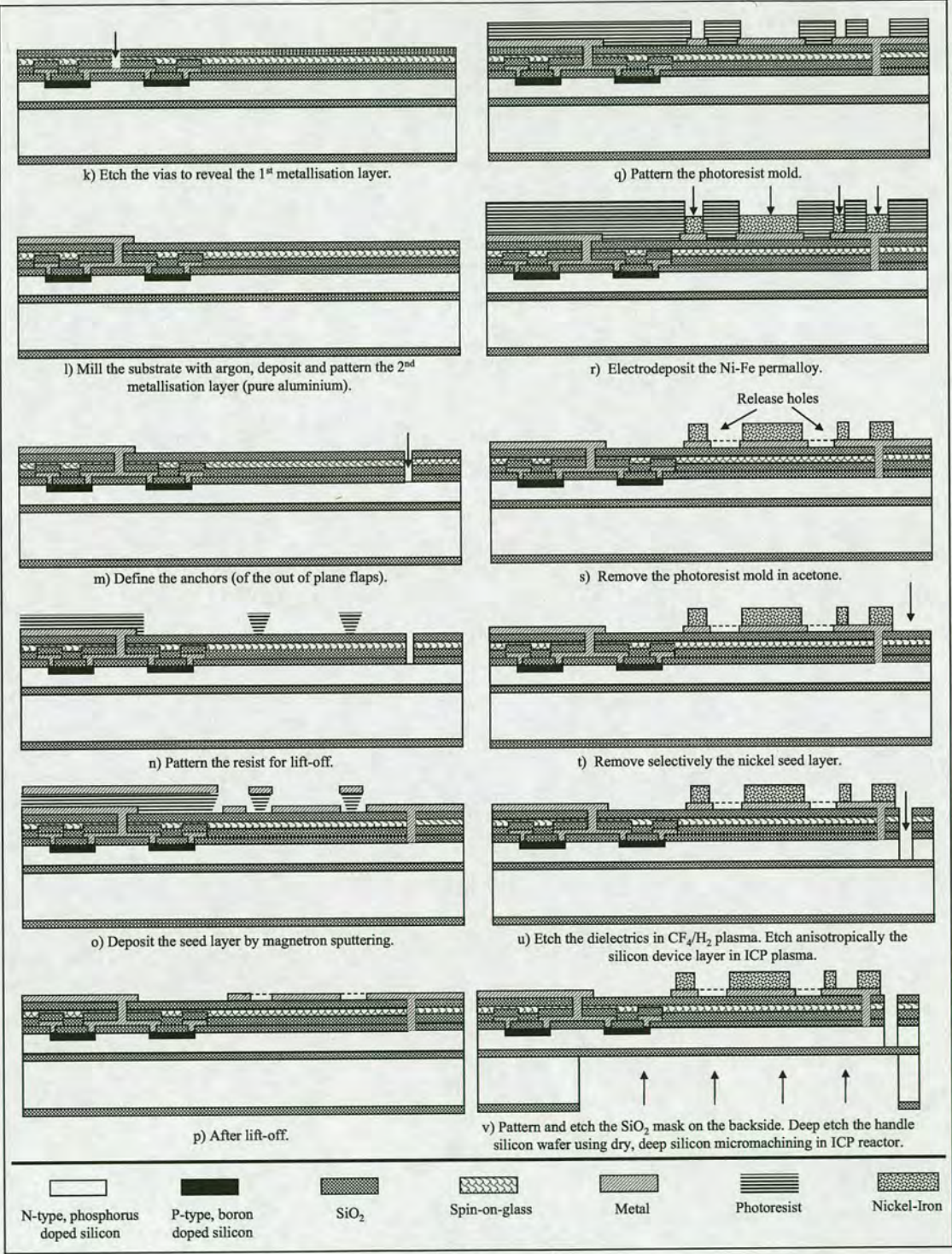
Appendix C

Fabrication process flow for the wind sensor



(a) Steps a - j

Figure C.1: Complete fabrication process flow for the wind sensor.



(b) Steps k - v

Figure C.1: Complete fabrication process flow for the wind sensor.

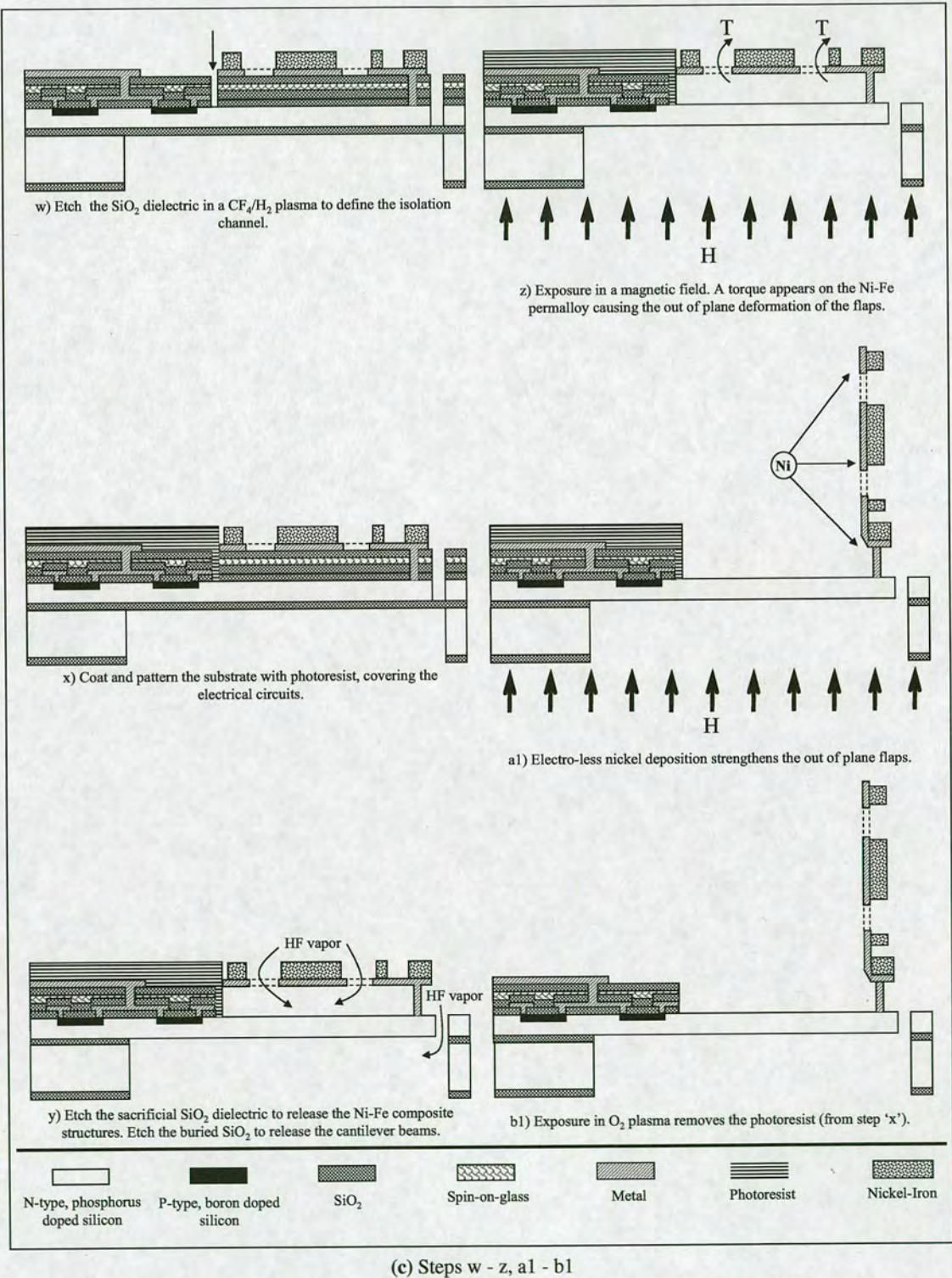


Figure C.1: Complete fabrication process flow for the wind sensor.

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